640 × 480 Real-Time Range Finder Using High-Speed Readout Scheme and Column-Parallel Position Detector

Yusuke Oike†, Makoto Ikeda†‡, and Kunihiro Asada†‡

†Dept. of Electronic Engineering, University of Tokyo
‡VLSI Design and Education Center (VDEC), University of Tokyo
7–3–1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
Phone: +81-3-5841-6719, Fax: +81-3-5841-8912
E-mail: {y-oike, ikeda, asada}@silicon.u-tokyo.ac.jp

Abstract

In this paper, we present the first real-time range finder with the capability of VGA (640 × 480) resolution based on a light-section method. We propose an adaptive thresholding circuit and column-parallel time-domain approximate ADCs to realize high-speed readout for real-time range finding. Sub-pixel position calculation based on intensity profile by the readout scheme achieves high-accuracy range finding. A column-parallel position detector suppresses redundant data transmission for a real-time measurement system.

Keyword: CMOS Image Sensor, Range Finder, Real Time, VGA, Light Section Method

Introduction

In recent years we often see 3-D computer graphics in movies and televisions, and handle them interactively using personal computers and video game machines. Latest and future 3-D applications require both higher pixel resolution for accurate range finding and higher frame rate for real time, not only just 3-D image. Fig.1 shows a structure of 3-D measurement system based on a light-section method. The system allows highly accurate range finding by simple triangular calculation. It, however, requires thousands of images every second for real-time 3-D measurement. For example, a 1024 × 1024 range map in video rate needs 30k fps. It is difficult for a standard readout architecture such as CCD. Even the high-speed CMOS APS using column-parallel ADCs [1] realizes 500 fps at most.

Some position sensors for the fast range finding are reported in [2]–[4]. The sensor using a row-parallel winner-take-all (WTA) circuit [2] can acquire a 64 × 64 range map in 100 range_map/sec. Its pixel size can be smaller than [3] due to the row-parallel architecture. The pixel resolution, however, is limited by the precision of the current-mode WTA circuit. It is difficult to realize enough high frame rate for real time with high pixel resolution. The sensor using pixel-parallel architecture [3] can acquire a 192 × 124 range map in video rate. It has a large circuit for frame memories and an ADC in pixel. Therefore they developed 160 × 120 3-D imager with analog frame memories out of a pixel array [4]. It makes a pixel circuit smaller and realizes high resolution as a QVGA color imager. It, however, sacrifices range finding rate and it is also difficult to get 3-D image in real time with higher pixel resolution.

In this paper, we present the first real-time range finder with the capability of VGA (640 × 480) resolution based on a light-section method. We propose two techniques for high-resolution and real-time range finding: a high-speed readout scheme and a column-parallel position detector. The high-speed readout scheme using adaptive thresholding and time-domain approximate ADC achieves high frame rate for real-time range finding and high range accuracy due to sub-pixel position calculation. In addition, it allows to use a standard and compact pixel circuit for high pixel resolution. The column-parallel position detector suppresses redundant data transmission for a real-time measurement system. 128 × 128 prototype sensor using our basic idea [5] shows that it has a potential for real-time range finding with very high pixel resolution such as VGA and more. Now a 640 × 480 range finder using these techniques has been developed and successfully tested. The measurement results of our new range finder and comparisons among the previous designs are shown.

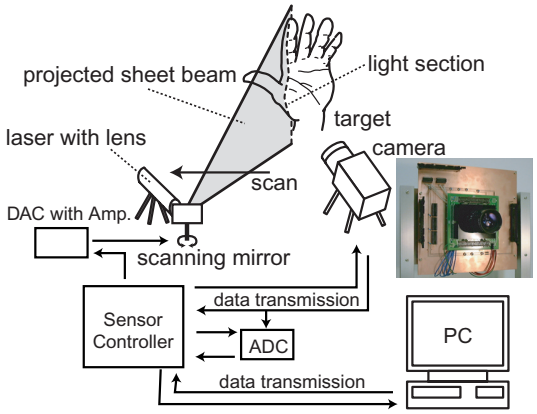

Fig. 1 3-D Measurement System Based on Light-Section Method.

Sensor Architecture and Circuit

Fig.2 shows the proposed sensing procedure for high-speed position detection. For 2-D imaging, all pixels are accessed using raster scan. On the other hand, a row line is accessed using the high-speed readout scheme, which is realized by adaptive thresholding and time-domain approximate ADCs (TDA-ADCs) in 3-D mode (a). Some pixels in a row line, where a strong light incidents, are detected for the location of the projected sheet beam when the pixel value is over the threshold level decided by dark pixel values adaptively (b). The pixel values over the threshold level are converted to digital by column-parallel TDA-ADC (c). The adaptive thresholding and the approximate ADC are carried out at the same time as dynamic pixel value reading. The results of the adaptive thresholding are transferred to a binary-tree priority encoder (PE) to get the left and right edge addresses of the detected pixels (d). The next stage outputs the intensity profile of the detected pixels using the results of the priority decision circuit (e).

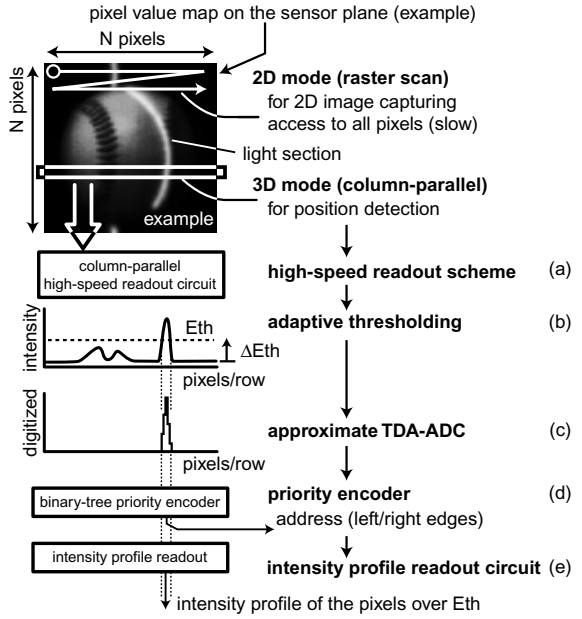

Fig. 2 Sensing Procedure for High-Speed Position Detection.

A. *High-Speed Readout Scheme*

Fig.3 shows a structure of high-speed readout scheme. In the present architecture, a pixel circuit can be the same as the 3-transistor CMOS APS [1]. This pixel structure realizes a small pixel area and high pixel resolution in general. In 2-D mode, PC is set to low and SW is set to low so that pixels work as the conventional APS. In 3-D mode, SW is set to high and column lines are precharged by giving a negative pulse signal to PC. After a row line is selected, the column outputs V_{col} begin to decrease depending on each pixel value as shown in Fig.3(a). Namely V_{col2} associated with pixels of a strong incident light is decreasing more slowly and its column output CMP_2 is enabled later as shown in Fig.3(b).

B. *Adaptive Thresholding Circuit*

In general, the conventional position sensor detects the pixels of stronger intensity than the fixed threshold intensity. In our sensing scheme, the threshold intensity E_{th}, shown in Fig.2 (b), is decided adaptively by the weakest intensity in each row as shown in Fig.3 (c). The common trigger signal COM is initiated by the column output of the darkest pixel. It propagates to the first stage of column-parallel latch sense amplifiers (SAs) through a delay T_{th}. The delayed signal $DCK0$ latches the column outputs CMP in parallel, that is, it detects late-arrival column outputs. The late-arrival stands for the pixel of strong intensity. The first delay T_{th} keeps a threshold margin ΔE_{th}, shown in Fig.2 (b), from the darkest level in time domain. The results ACT of the first stage latch indicates whether a pixel is activated or not. They are transferred to the next priority encoder stage.

C. *Time-Domain Approximate ADC*

The intensity of the activated pixels can be acquired by a column-parallel time-domain approximate ADC (TDA-ADC). The common trigger signal COM continues to propagate through a delay T_{res} as SA clock signals DCK_n as shown in Fig.3(c). DCK_n latches the column outputs CMP at the n-th stage one after another as shown in Fig.3(b). The arrival timing

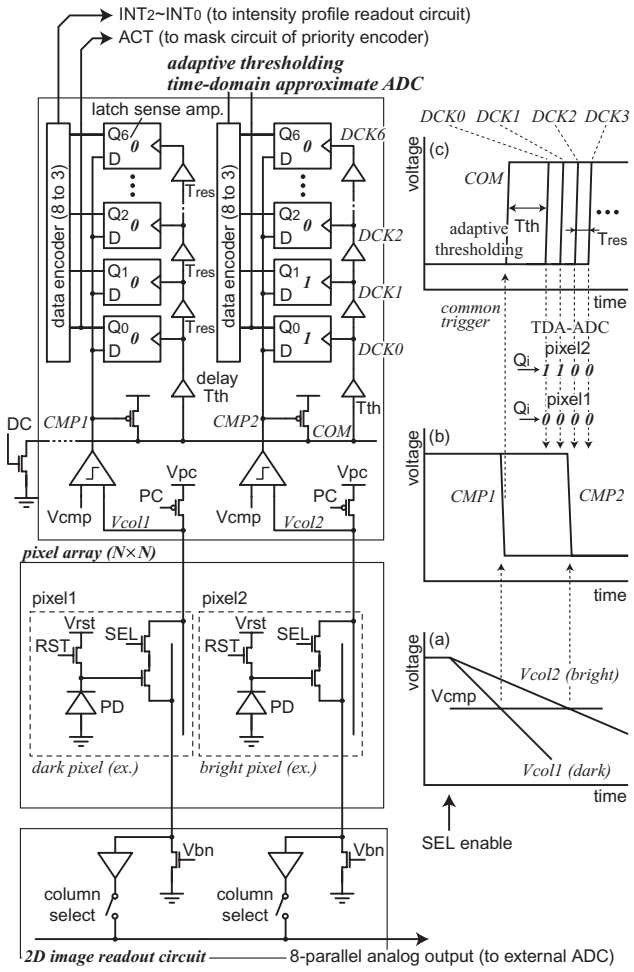

Fig. 3 Schematic and Operation of high-speed readout scheme.

of a column output depends on the pixel value, so the results INT_2–INT_0 of TDA-ADC show an approximate intensity of each selected pixel normalized by the darkest pixel in the row.

The high-speed readout scheme provides the locations of the detected pixels and its intensity profile simultaneously. Fig.4 shows its timing diagram. Using the location of active pixels, the intensity profiles are read out quickly and utilized for off-chip gravity center calculation for high sub-pixel accuracy.

D. *Column-Parallel Position Detector*

Fig.5 shows a schematic of the binary-tree priority encoder (PE), which receives the adaptive thresholding results ACT. It consists of a mask circuit, a binary-tree priority decision circuit and an address encoder. At the mask circuit, ACT_n is compared with the neighbors ACT_{n+1} and ACT_{n-1} to detect the left and right edges. The priority decision circuit receives PRI_IN_n from the mask circuits and generates the output at the minimum address of activated pixels, for example PRI_OUT_3 in Fig.5. The addresses of the left and right edges are encoded at the address encoder. After the first-priority edge has been detected, the edge is masked by PRI_OUT_n and MCK. And then the location of the next priority of activated pixels is encoded. Our improved priority decision circuit keeps high speed in large input number due to a binary-tree structure and a compact circuit cell. Its delay increases in proportion to $\log(N)$, where N is input number.

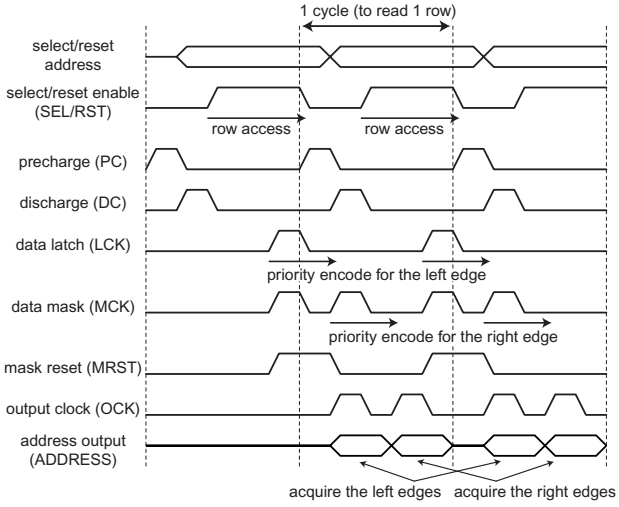

Fig. 4 Timing Diagram of the High-Speed Readout Scheme.

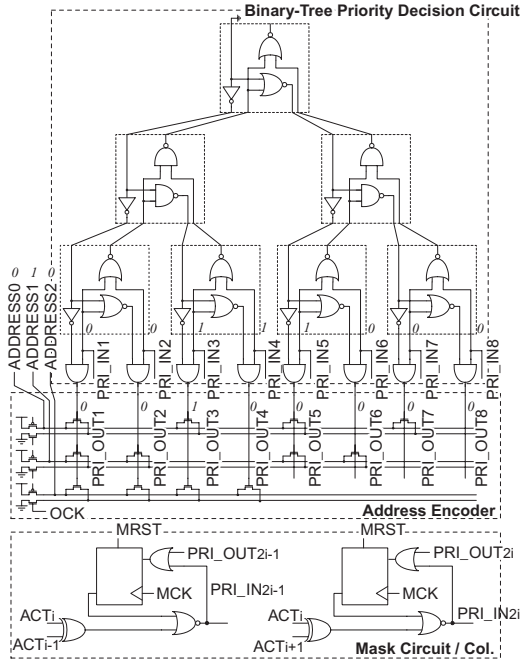

Fig. 5 Schematic of the Binary-Tree Priority Encoder.

Chip Implementation

We have designed and fabricated a 640 × 480 range finder using the present architecture and circuit in 0.6 μm CMOS process[1]. Fig.6 shows its chip microphotograph and components. The sensor has a 640 × 480 pixel array, row select and reset decoders, 2-D image readout circuit, column-parallel TDA-ADCs, a 640-input priority encoder and an intensity profile readout circuit in 8.9 mm × 8.9 mm die size. The pixel has a photo diode and 3 transistors. Its area is 12 μm × 12 μm with 29.5% fill factor. Table I shows the specifications of the fabricated sensor.

[1]The sensor in this study has been designed with CAD tools of Synopsys Inc. and Cadence Design Systems Inc., and fabricated through VLSI Design and Education Center (VDEC), University of Tokyo in collaboration with Rohm Corp. and Toppan Printing Corp.

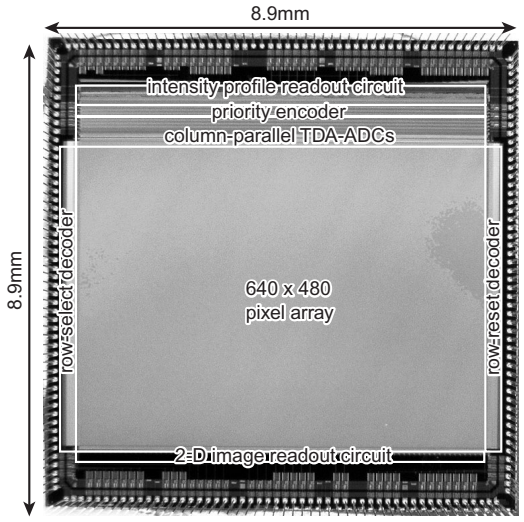

Fig. 6 Chip Microphotograph.

TABLE I Specifications of the Fabricated Sensor.

Process	0.6 μm CMOS 3-metal 2-poly-Si
Die size	8.9 mm × 8.9 mm
# of pixels	640 × 480 pixels (VGA)
# of transistors	1.12M transistors
Pixel size	12.0 μm × 12.0 μm
# of trans. / pixel	3 transistors
Fill factor	29.54 %

Measurement Results

The fabricated range finder has been mounted on a test board in 3-D measurement system based on a light-section method as shown in Fig.1. The 3-D measurement system is composed of the camera, a laser (wavelength 665 nm) with a rod lens for beam extension, a scanning mirror with a DAC, an ADC for 2-D imaging, an FPGA for sensor control, and a PC for display.

A. *Frame Rate*

In 2-D imaging, 8 pixel values are readout in parallel and it takes 2 μs. The maximum 2-D imaging speed is 13 fps (frames/sec) using 8-parallel high-speed external ADCs. It has a potential of higher speed of 2-D imaging since it is easy to implement the conventional readout techniques for 2-D imaging in our sensor architecture.

In 3-D imaging, the precharge voltage V_{pc} is set to 3.5 V and the compared voltage V_{cmp} is set to 3.0 V. Activated pixels in a row line are accessed and detected in 50 ns. The delay time of the priority encoder stage is 17.2 ns for the left and right edges. The readout time of the intensity profile is 21.5 ns. Their stages are pipelined. Therefore the location of the projected sheet beam is acquired in 24.0 μs. The range finder realizes 65.1 range_maps/sec in VGA pixel resolution. Fig.7 shows the pixel resolution and 3-D imaging speed of our present range finder with a comparison among the previous designs.

B. *Range Accuracy*

Fig.8 shows measured distances of a white flat board by the present range finder. The standard deviation of measured error is 0.26 mm and the maximum error is 0.87 mm at a distance of 1170 mm – 1230 mm by gravity center calculation using

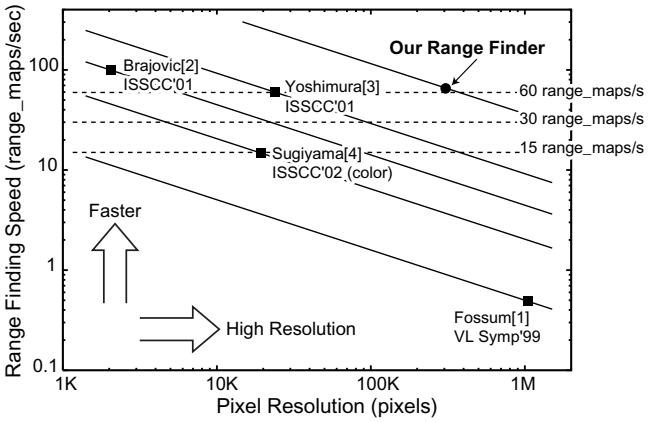

Fig. 7 Range Finding Speed and Pixel Resolution.

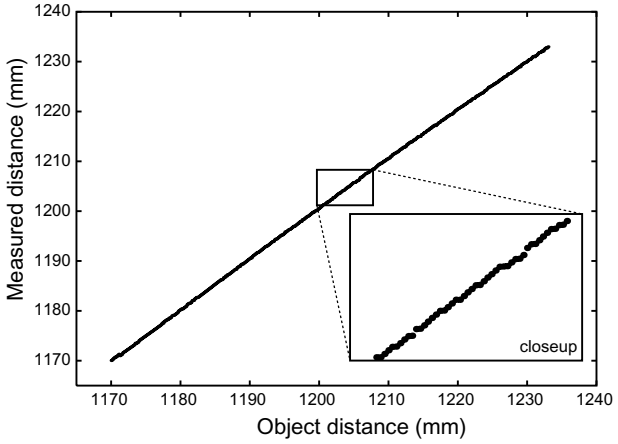

Fig. 8 Measured Range Accuracy.

TABLE II Performance of the Present Range Finder.

Power supply voltage	5.0 V
Power dissipation	305 mW (at 10 MHz operation)
Max. 2-D imaging rate	†13.0 frames/sec
Max. position detection rate	41.7k lines/sec
Max. range finding rate	65.1 range_maps/sec
Range accuracy (max. error)	0.87 mm at a distance of 1200 mm

†limited by off-chip ADC

an acquired intensity profile. For comparison, the standard deviation of measured error is 0.54 mm and the maximum error is 2.13 mm by the conventional binary-based position calculation. An intensity profile could be distorted by device fluctuation, but the measurement results show that the present range finder achieves higher accuracy than the conventional position sensor using a binary image.

C. *Measured Images*

Fig.9 shows measured images by the present range finder. Fig.9(a) is a captured 2-D image of a hand. Fig.9(b)–(d) are its range maps. The brightness of the range maps represents the distance from the range finder to the target object. The range data has been already plotted in 3-D space, so it can be rotated freely as shown in Fig.9(b)–(d). Fig.9(e) is a wire frame reproduced by the measured range data and Fig.9(f) is a closeup of Fig.9(e). The measured images show that our range finder with VGA pixel resolution realizes high-resolution 3-D imaging.

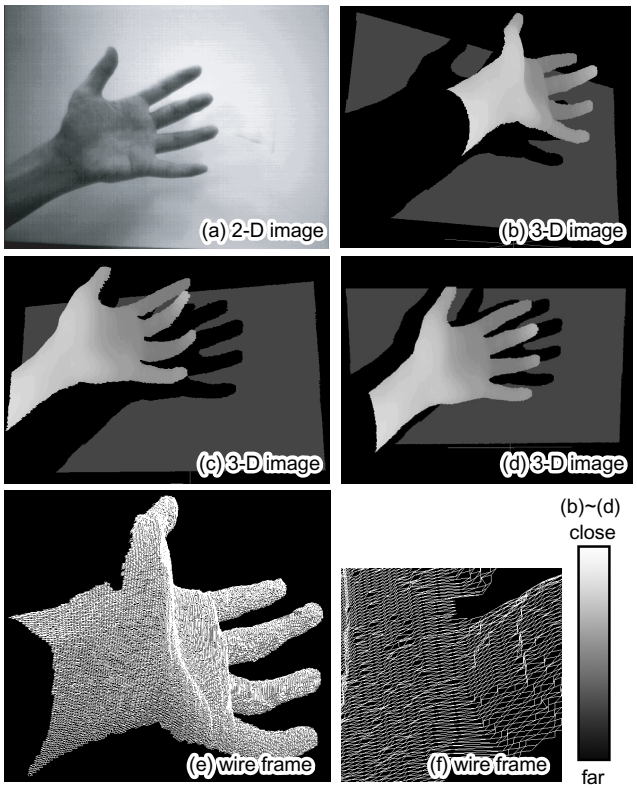

Fig. 9 Measurement Results of the Present Sensor.

Conclusions

A 640 × 480 real-time range finder using a high-speed readout scheme and a column-parallel position detector has been presented. It is the first range finder based on a light-section method to realize VGA pixel resolution and real-time range finding. Our high-speed readout scheme realizes to use a standard and compact pixel circuit and to get the location and the intensity profile of an incident sheet beam quickly. The column-parallel position detector suppresses redundant data transmission for a real-time measurement system. The maximum range finding speed is 65.1 range_maps/sec. The maximum range error is 0.87 mm and the standard deviation of error is 0.26 mm at 1200 mm distance due to an intensity profile. A 2-D image and a high-resolution 3-D image have been acquired by the 3-D measurement system using the fabricated range finder.

References

[1] A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E. R. Fossum, "A High Speed, 500 Frames/s, 1024 × 1024 CMOS Active Pixel Sensor," *IEEE Symp. VLSI Circuits Dig. of Tech. Papers*, 1999, pp. 137-138.

[2] V. Brajovic, K. Mori and N. Jankovic, "100 frames/s CMOS Range Image Sensor," *ISSCC Dig. of Tech. Papers*, pp. 256 – 257, 2001.

[3] S. Yoshimura, T. Sugiyama, K. Yonemoto and K. Ueda, "A 48k frame/s CMOS Image Sensor for Real-time 3-D Sensing and Motion Detection," *ISSCC Dig. of Tech. Papers*, pp. 94 – 95, 2001.

[4] T. Sugiyama, S. Yoshimura, R. Suzuki and H. Sumi, "A 1/4-inch QVGA Color Imaging and 3-D Sensing CMOS Sensor with Analog Frame Memory," *ISSCC Dig. of Tech. Papers*, pp. 434 – 435, 2002.

[5] Y. Oike, M. Ikeda and K. Asada, "Smart Sensor Architecture for Real-Time and High-Resolution Range Finding," *in Proc. European Solid-State Circuit Conference*, pp. 105 – 108, 2002.