A 375 × 365 High-Speed 3-D Range-Finding Image Sensor Using Row-Parallel Search Architecture and Multisampling Technique

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***Abstract*—A high-speed three-dimensional (3-D) image sensor for a 1000 range maps/s 3-D measurement system based on a light-section method is presented. It employs a row-parallel search architecture to achieve a high-speed frame access rate for the detection of activated pixels on the focal plane. The row-parallel search operation is carried out using chained search circuits embedded in a pixel. Moreover, we propose a row-parallel address acquisition technique using a bit-streamed column address flow. Row-parallel processors receive the bit-streamed column address and calculate the center position of activated pixels. The pipelined operations enable a multisampling technique that improves the resolution of pixel detection. A 375 × 365 3-D image sensor using the present architecture has been designed in a one-poly five-metal 0.18-μm standard CMOS process and successfully tested. It attains a frame access rate of 394.5 kHz with four samplings, which corresponds to 1052 range maps/s. The multisampling operation improves the sub-pixel resolution to around 0.2 pixels and achieves a range accuracy of less than 1.10 mm at a target distance of 600 mm.**

***Index Terms*—CMOS image sensor, high range accuracy, high speed, light-section method, multisampling method, range finder, row parallel architecture, 3-D image sensor.**

I. Introduction

A HIGH-SPEED and high-resolution three-dimensional (3-D) imaging system has a wide variety of applications including gesture recognition, depth-key object extraction, position adjustment, computer vision and security systems. In recent years, we have often seen 3-D computer graphics in movies and televisions and handled them interactively using personal computers and video game machines. Moreover, ultra-high-speed range finding provides the possibility of additional applications such as shape measurement of structural deformation and destruction, quick inspection of industrial components, observation of high-speed moving objects, and fast visual feedback systems in robot vision.

Some 3-D range-finding image sensors have been presented for 3-D imaging applications based on the stereo-matching method [1], [2], the time-of-flight method [3]–[7], and the light-section method [8]–[13]. The stereo-matching method provides a simple system configuration with two or more cameras. The stereo-matching processing, however, requires a huge computational effort with a high pixel resolution, and the range resolution and accuracy depend on target surface patterns. It is also difficult for the time-of-flight method to provide high range accuracy due to the limitations on the phase detection speed of a pulsed light. On the other hand, the light-section method is capable of high-accuracy range finding and it is most suitable for precision shape analysis. A typical configuration of light-section range finding is shown in Fig. 1(a). A sheet laser beam is projected and scanned on a target object. An image sensor detects the positions of the reflected beam on the sensor plane. 3-D range data are calculated by the beam projection angle α_p and the beam incidence angle α_i based on triangulation as shown in Fig. 1(b). The beam incidence angle can be acquired by the position of the incident beam on the sensor. Therefore many frames are necessary for a 3-D range image during the beam scanning. For example, a 1000 range maps/s 3-D measurement system with a practical pixel resolution requires over 100-kHz frame access rate. It is difficult for conventional image sensors to realize such a high-speed frame access. Fig. 2 plots the trend of range finding speed and pixel resolution in the state-of-the-art high-speed image sensors [14], [15] and light-section 3-D range finders [10]–[13]. It also shows examples of high-speed range finding applications. The conventional 3-D range finders have achieved 40–50 kHz frame access rate for real-time 3-D imaging. However, the target area of 1000 range maps/s requires around 400-kHz frame access rate. Therefore, we have presented a concept of a row-parallel search architecture on the focal plane and demonstrated the possibility of 1000 range maps/s range finding with a practical pixel resolution [16].

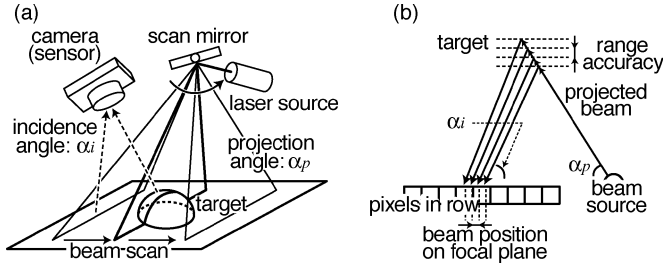

Fig. 1. Triangulation-based light-section range finding system. (a) System configuration. (b) Relation between range accuracy and beam position on the focal plane.

This paper presents a 3-D image sensor with 375 × 365 pixels for a 1000 range maps/s 3-D measurement system based on the light-section method, which was reported in part at the IEEE

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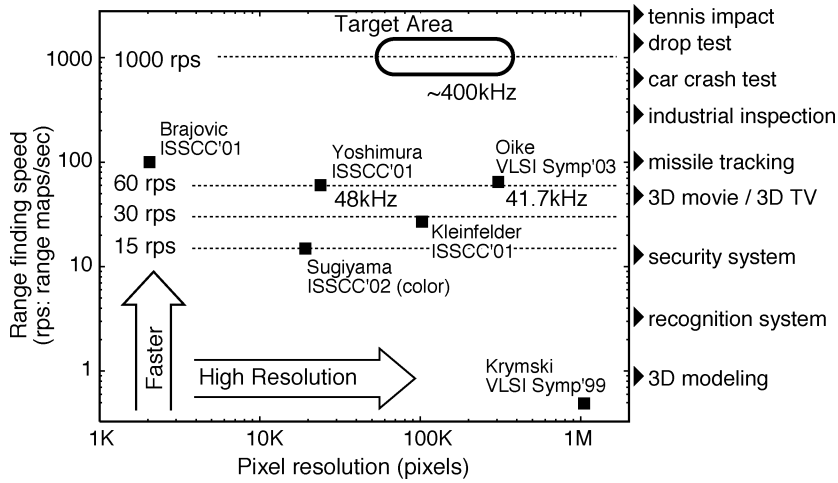

Fig. 2. Previous works and application examples.

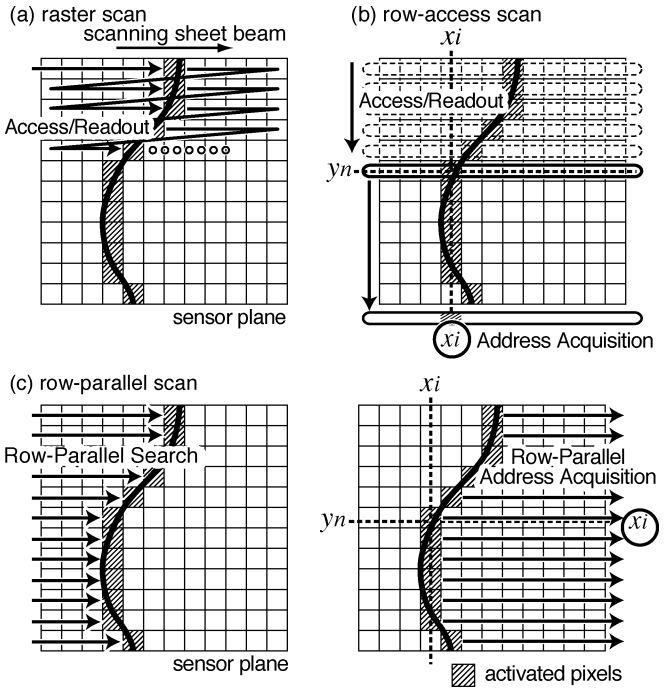

Fig. 3. Frame access methods. (a) Raster scan. (b) Row-access scan. (c) Row-parallel scan.

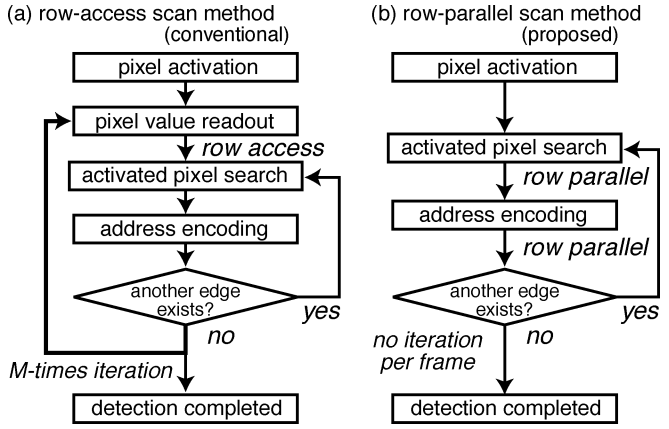

Fig. 4. Position detection flow. (a) Conventional row-access scan method with M row lines. (b) Proposed row-parallel scan method.

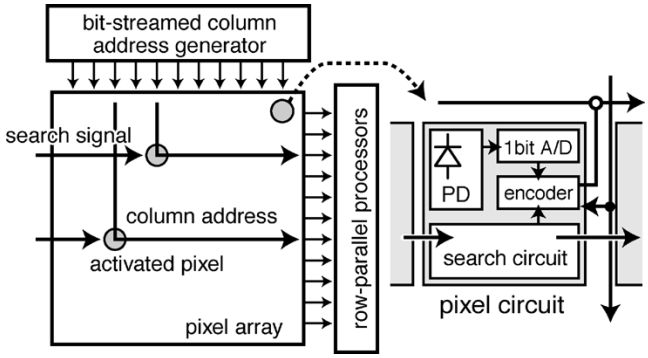

Fig. 5. Row-parallel position detection architecture implemented on the sensor plane.

ISSCC 2004 [17]. The row-parallel search architecture is implemented in three pipelined stages with a new multisampling function. The separated stages of photo integration, position detection, and data readout enable a high-speed frame access rate with multiple samplings. The multisampling technique improves the sub-pixel resolution of position detection on the focal plane for high range accuracy.

Section II presents the concept of a row-parallel search architecture. Circuit configurations and operations are described in Section III. Section IV introduces the multisampling technique with theoretical estimation of the improved sub-pixel resolution. Then, Section V shows the chip specification of a designed 3-D image sensor. The measurement results are discussed in Section VI. Finally, Section VII concludes this paper.

II. Row-Parallel Position Detection Architecture

A. Concept of Row-Parallel Search Architecture

Conventional image sensors typically employ a raster scan method or a row-access scan method. The raster scan method accesses all the pixels sequentially for a few activated pixels on the focal plane as shown in Fig. 3(a). The row-access scan method also needs to access all the pixel values. In row-access image sensors such as [11]–[13], the activated pixels in a row

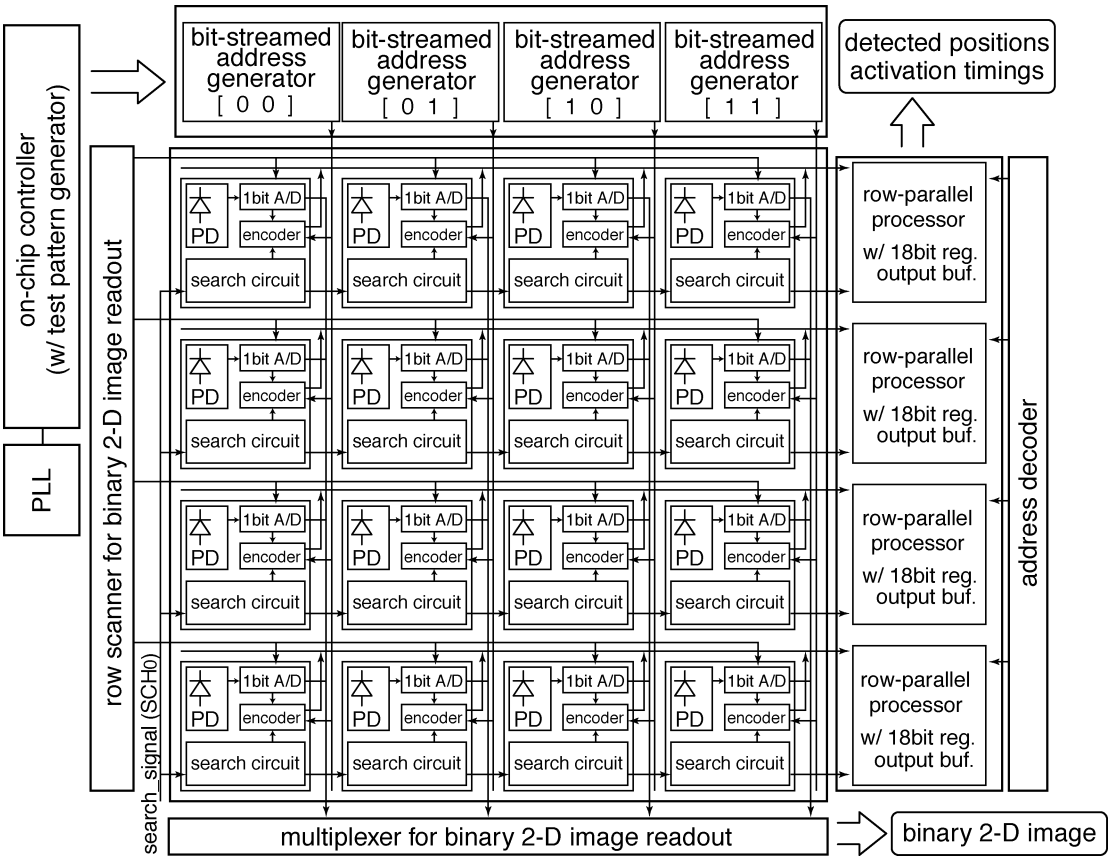

Fig. 6. Simplified block diagram of 4 × 4 pixels.

line can be scanned and detected in a column parallel fashion as shown in Fig. 3(b). Therefore, the row-access scan method is more suitable for high-speed position detection than the raster scan method. Fig. 4(a) shows the position detection flow of the row-access scan method. First some pixels are activated by a strong incident beam. Then the pixel values in a row line are read out. The activated pixels are scanned and detected in column parallel. The left and right edge addresses of consecutively activated pixels are acquired. If another incident beam exists in the row line, the search and address encoding operations are repeated. After that, the next row line is accessed and the pixel values are read out again. The access and search operations are repeated in proportion to the number of row lines. The access rate, limited to about 50 kHz, becomes the bottleneck.

Fig. 3(c) shows the proposed row-parallel scan method on the focal plane. In the row-parallel scan method, activated pixels in every row line are simultaneously scanned in row parallel. Then the addresses are acquired also in row parallel. Therefore there is no access iteration in proportion to the pixel resolution as shown in Fig. 4(b).

B. Block Diagram of Row-Parallel Scan Sensor

The present row-parallel architecture is implemented on the sensor plane as shown in Fig. 5. The row-parallel search operation is carried out by a chained search circuit embedded in each pixel. Search signals are provided from the left part of the sensor. They propagate from one pixel to the next pixel one after another via the in-pixel search circuit in a row parallel fashion. Then, the search propagation is interrupted at the first-encountered active pixel in each row line. In terms of address acquisition, it is impractical to implement an address encoder in every row line since a regularly spaced array structure is necessary for an image sensor. If a standard address encoder is implemented in each pixel, it requires many transverse wires per row as well as a large circuit area per pixel. We propose a bit-streamed column address flow for row-parallel address acquisition that enables compact circuit implementation. Column address streams are injected at the top part of the sensor in column parallel, and change their directions at pixels detected by the search circuits. The address acquisition scheme requires just one vertical wire per column and one transverse wire per row, which is suitable for a high-resolution pixel array. Each pixel includes a photo detector, a 1-bit A/D converter, a search circuit, and part of an address encoder.

Fig. 6 shows an overview of the row-parallel scan image sensor simplified to 4 × 4 pixels. It consists of a pixel array, bit-streamed column address generators at the top, row-parallel processors with data registers and output buffers on the right, a row scanner on the left, and a multiplexer at the bottom. These components are controlled by an on-chip sensor controller with a phase-locked loop (PLL) module. Pixels in a row line are connected with neighbor pixels by a search signal path. Column address streams are provided from the address generators to each vertical wire. Then the bit-streamed address signals are

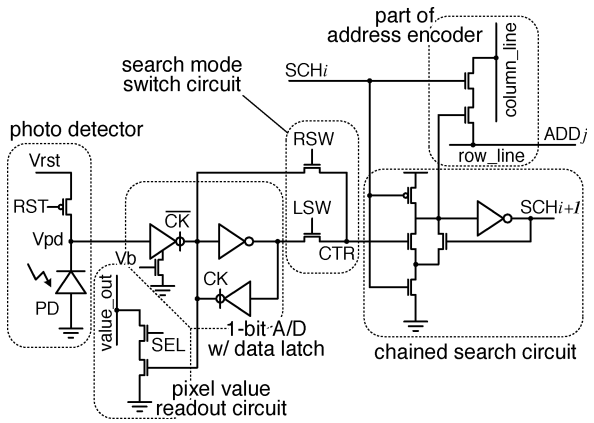

Fig. 7. Schematic of a pixel circuit.

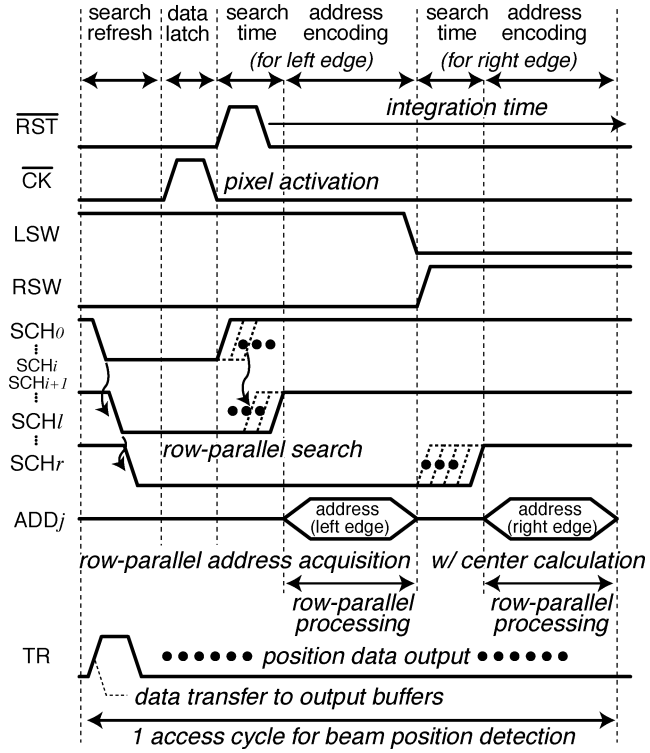

Fig. 8. Timing diagram of a pixel circuit.

injected to horizontal wires at the detected pixels. The row-parallel processors receive the bit-streamed address signals and the search completion signals from the right pixels in each row.

III. Circuit Configuration and Operation

A. Pixel Circuit Configuration

Fig. 7 shows the pixel circuit configuration with row-parallel position detection functions. It consists of a photo detector with a reset circuit, a 1-bit A/D converter with a latch circuit, a pixel value readout circuit, a search mode switch circuit, a chained search circuit, and part of an address encoder. The voltage V_{pd} is set to a reset voltage V_{rst} by *RST*. The 1-bit A/D converter receives V_{pd} and determines the pixel value. The voltage V_{pd} becomes a low level in case of an active pixel with strong incident intensity. Therefore, it provides "0" for an active pixel value, and

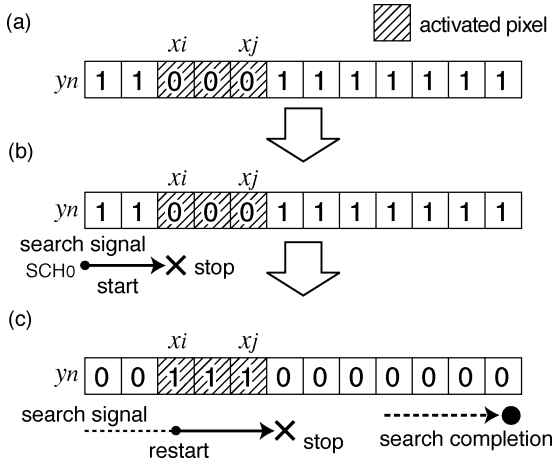

Fig. 9. Procedure of row-parallel activated pixel search. (a) Pixel activation; (b) search left edge; (c) invert all pixel values and search right edge.

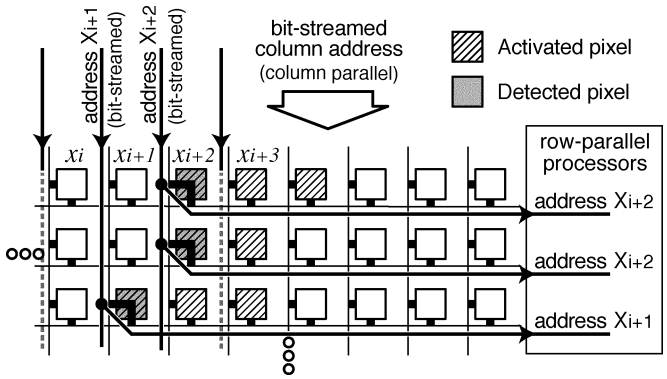

Fig. 10. Bit-streamed column address flow for row-parallel address acquisition.

"1" for an inactive pixel value. A transistor biased by V_b reduces the short-circuit current and controls the threshold level of A/D conversion. The pixel value readout circuit provides a binary image for functional tests. The search mode switch circuit and the chained search circuit are devoted to a row-parallel search for activated pixels. The address encoding section connects a column address line with a row address line. The row-parallel search and address acquisition functions are described in detail in the next sections.

B. Row-Parallel Search Operation

The row-parallel search operation is carried out using a chained search circuit embedded in each pixel. First, it detects the left edge of consecutively activated pixels in each row. Fig. 8 shows a timing diagram of the pixel circuit. Fig. 9 shows the procedure of the row-parallel search for activated pixels. The search mode switch circuit, which is implemented by a pass-transistor XOR, provides a control signal *CTR* for the search circuit. For the left edge detection, *LSW* and *RSW* are set to a high level and a low level, respectively. As the result of pixel activation, the activated pixel values are "0" and the others are "1"' as shown in Fig. 9(a). A search signal SCH_0 is provided to the left pixel in each row line. It passes through inactive pixels one after another via the in-pixel search circuits since the control signal *CTR* is set to a high level. The search

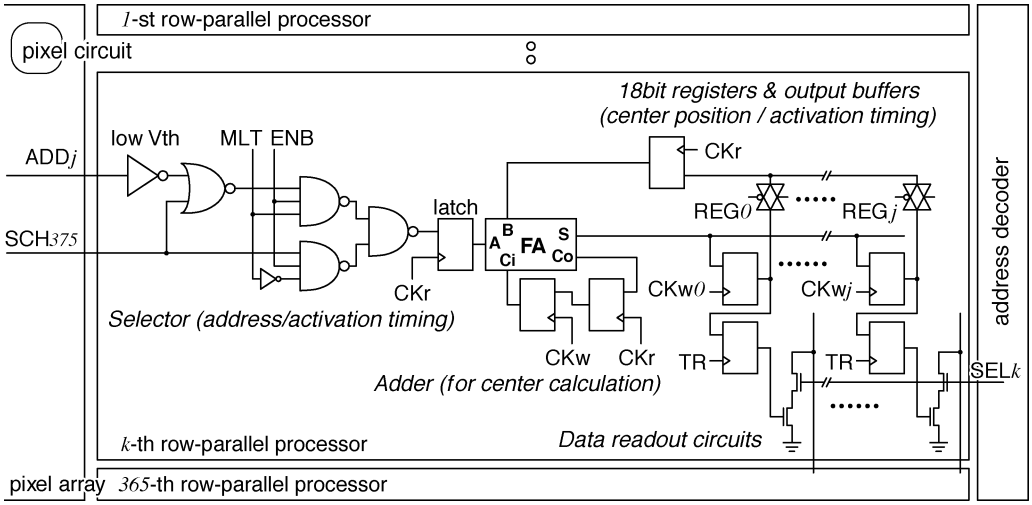

Fig. 11. Schematic of a row-parallel processor.

signal propagation is interrupted at the first-encountered active pixel as shown in Fig. 9(b), that is, it detects the left edge of consecutively activated pixels. After row-parallel address acquisition, *LSW* turns OFF and *RSW* turns ON. All the pixel values are inverted for the right edge detection as shown in Fig. 9(c). Namely, the active pixel values change to "1" and the interrupted search signal immediately starts again from the left edge. It passes through active pixels one after another and then stops at the next pixel of the right edge.

The worst delay of the search operation is the signal propagation delay through all the pixels in a row line. Therefore the search clock cycle is determined by the worst-case delay. The center position of incident beam can be calculated by the left and right edge addresses. The number of search cycles is the same regardless of the number of consecutively activated pixels. If another activated pixel exists on the same row, all the pixel values can be inverted again by switching *LSW* and *RSW*. The search operation restarts from the detected right edge to the next left edge. Therefore the row-parallel search operation is capable of position detection for multiple incident beams due to the search continuation. The last search signal SCH_n from the right pixel indicates whether no activated pixel exists in each row as a search completion signal.

C. Row-Parallel Address Acquisition

Fig. 10 shows a bit-streamed column address flow for row-parallel address acquisition. A column address line is connected to a row address line by part of an address encoder in the detected pixel. The row-parallel address acquisition needs just 2 pass transistors in a pixel as shown in Fig. 7. At the detected left edge, SCH_l from the previous pixel becomes a high level, but the next search signal SCH_{l+1} is still a low level since the search signal propagation is interrupted. Therefore, both inputs, SCH_i and $\overline{SCH_{i+1}}$, are set to a high level at the detected pixel. A bit-streamed address signal is then provided from a column address line to a row address line via the two pass transistors. The column address streams never conflict with each other in the same row line since the left or right edge is detected by the row-parallel search in each row. The bit-streamed address signals are injected from the LSB to the MSB, and then they are received by the row-parallel processors.

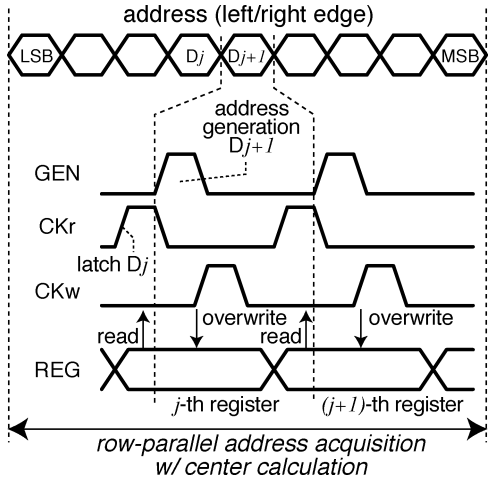

Fig. 12. Timing diagram of a row-parallel processor.

D. Row-Parallel Processing

The range-finding image sensor has row-parallel processors that receive bit-streamed address signals ADD_j and search completion signals SCH_{375} in each row. Fig. 11 shows a schematic of the row-parallel processor. It consists of a selector with a signal receiver, a full adder, 18-bit registers, 18-bit output buffers, and data readout circuits. The selector switches the processing functions, which are an address acquisition mode and an activation counting mode. Fig. 12 shows a timing diagram of the row-parallel processor. A bit-streamed address signal is received by a low-threshold inverter because the address signal cannot swing to the supply voltage due to pass transistors in a pixel. In a multisampling operation, the row-parallel processor counts the number of usable pixel activations by the search completion signal since an occasional search operation includes no activated pixel. The address acquisition mode and the activation counting mode are switched by *MLT*. The left edge

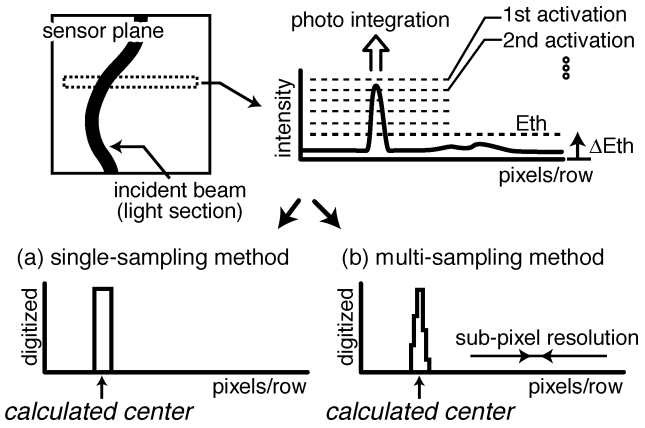

Fig. 13. Sub-pixel center position detection by multisampling method. (a) Single-sampling method. (b) Multisampling method.

address is stored in the registers. Then the right edge address is accumulated on the left edge address by CK_r and CK_w in sequential order from the LSB to the MSB. *ENB* is employed to disable the input of the full adder for carry accumulation in a multisampling operation. The accumulated address represents the center position of activated pixels. The results are transferred to the output buffers by *TR*, and then they are read out by SEL_k during the search operations for the next frame. The row-parallel processing is executed concurrently with the row-parallel address acquisition. The row-parallel processor has the capability to perform a multisampling operation due to the high-speed position detection.

IV. Multisampling Position Detection

Three-dimensional range data is calculated by the beam projection angle α_p and the incident angle α_i as shown in Fig. 1(b). The incident beam angle α_i is provided from the incident beam position on the focal plane. Therefore, the range resolution and accuracy depend on the resolution of position detection on the sensor. In other words, the sub-pixel resolution efficiently improves the range accuracy. A multisampling technique is implemented to acquire the intensity profile of incident beam for a fine sub-pixel resolution.

In a multisampling method, all the pixel values are updated repeatedly during the photo integration. Pixels with stronger incident intensity are activated faster and found many times in multiple samplings as shown in Fig. 13. In the conventional single sampling mode, the acquired data are binary, and so the sub-pixel resolution of calculated center position is 0.5 pixels as shown in Fig. 13(a). On the other hand, the number of samplings represents the scale of the intensity profile as shown in Fig. 13(b). Some scales provide a fine sub-pixel resolution of center position detection for range accuracy improvement. Fig. 14 shows a theoretical estimation of the sub-pixel resolution as a function of the number of samplings. A gaussian distribution is assumed as the beam intensity profile. The sub-pixel resolution is efficiently improved in 2–8 samplings. For example, a 4-sampling mode attains 0.2 sub-pixel resolution.

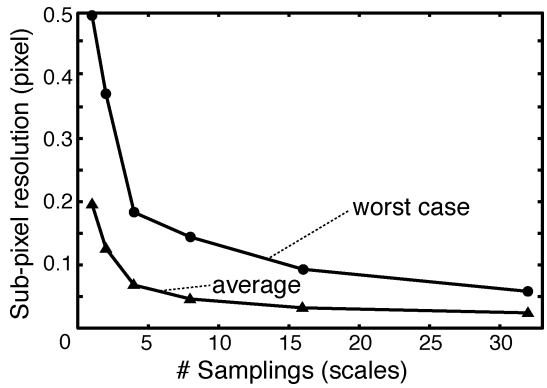

Fig. 14. Sub-pixel resolution as a function of the number of samplings.

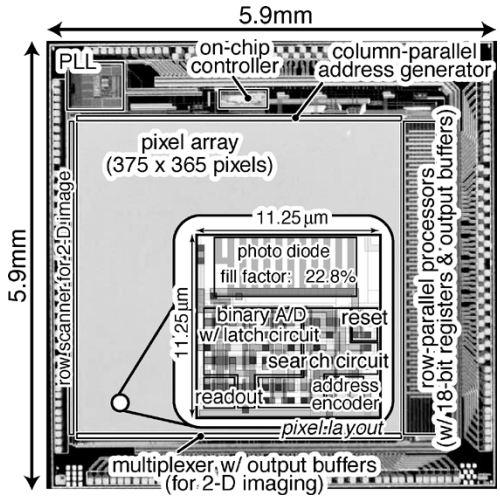

Fig. 15. Die microphotograph and pixel layout.

TABLE I
Chip Specifications

Process	1P5M 0.18 μm CMOS process
Die size	5.9 mm × 5.9 mm
Resolution	375 × 365 pixels
Pixel size	11.25 μm × 11.25 μm
Fill factor	22.8 %
Pixel configuration	1 PN-junction PD, 24 FETs / pixel
Total FETs	3.74 M transistors

V. Chip Implementation

A 375 × 365 3-D range-finding image sensor using the present row-parallel architecture has been designed and fabricated in a 0.18 μm standard CMOS process with 1-poly-Si 5-metal layers. The die size is 5.9 mm × 5.9 mm. Fig. 15 shows a chip microphotograph and a pixel layout. The sensor consists of a 375 × 365 pixel array, a column-parallel address generator, and row-parallel processors with 18-bit registers and output buffers. A row scanner and a column multiplexer are also implemented to acquire a binary 2-D image for test. The row-parallel operations are executed by an on-chip sensor controller with a PLL module. The implementation requires 3.74 million transistors. The supply voltage is 1.8 V. The pixel size is 11.25 μm × 11.25 μm with 22.8% fill factor. It consists of a PN-junction photo diode and 24 transistors. The photo diode is composed of n^+-diffusion and p-substrate. It is split into

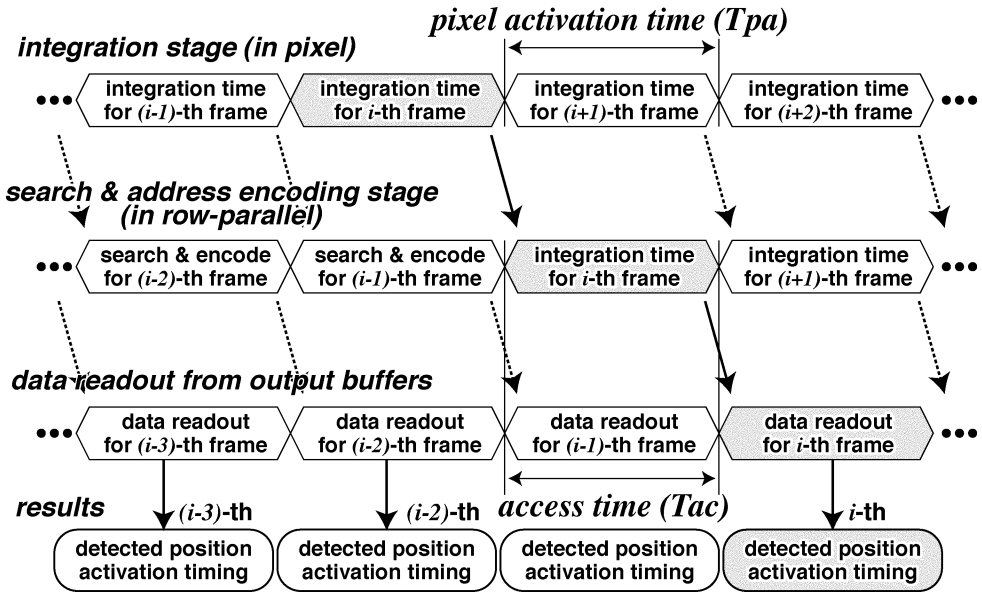

Fig. 16. Pipelined operation diagram.

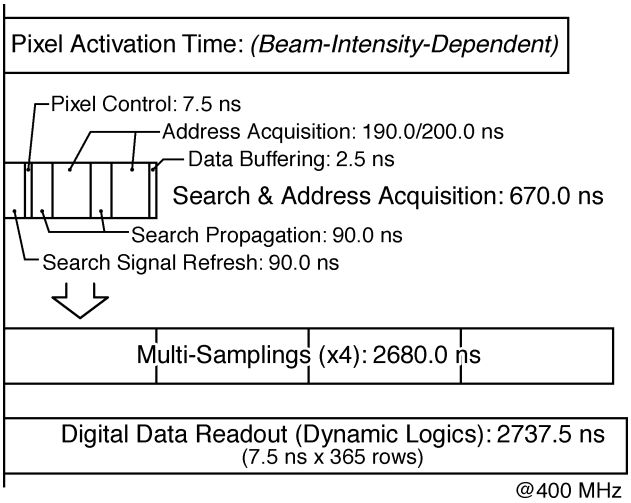

Fig. 17. Cycle time of activated pixel search and data readout.

several rectangular slices to improve the sensitivity since the present CMOS process has no option of silicide layer removal. Table I shows the chip specifications.

VI. Measurement Results

A. Frame Access Rate

The row-parallel position detection is pipelined in three stages on the sensor as shown in Fig. 16. The first stage is the photocurrent integration for pixel activation. The second stage is the row-parallel operation of activated pixel search and address acquisition. The last stage is the data readout operation from output buffers. The photocurrent integration period is called the pixel activation time. It depends on the incident beam intensity and the sensitivity of a photo diode. That is, the pixel activation time can be controlled by the beam intensity. On the other hand, the access time is limited by a search operation with address acquisition or a data readout operation. Therefore our principal aim is to achieve a short access time for high-speed position detection.

Fig. 17 shows a cycle time of each pipelined stage at a 400-MHz operation. The worst case of search signal propagation takes 90 ns. So the search path refresh and the search operations for the left and right edges each require 90 ns. The row-parallel address acquisition takes less than 200 ns in the worst case. The worst case of address acquisition occurs when all the detected pixels are placed on the same column because the load capacitance of a column address generator becomes largest and limits the injection speed of the bit-streamed column address signals. The total cycle time of search and address acquisition is 670 ns. The limiting factor of the access time is the digital readout stage from output buffers, which requires 2737.5 ns. Therefore, the search and address acquisition can be repeated four times in the data readout period while maintaining the frame access rate.

We have tested the maximum access rate of the designed sensor. The sensor allows user-specified pixel activation. The worst-case situation is set by an electrical pattern on the sensor plane. Fig. 18 shows measured waveforms of the worst-case frame access to an electrical test pattern at 432 MHz. Fig. 19 shows a data readout circuit and the test equipment that was used for probing the output signals. Output buffers in each row are selected by SEL_k. The position results are read out by the dynamic readout circuits where are precharged by *PRE*, and received by sense amplifiers that are synchronized with *SACK*. The reference voltage $V_{\rm ref}$ is set to 300 mV below the supply voltage. The output signals are probed with parasitic capacitances of C_{IN} and C_{PB}, which are 7 and 13 pF, respectively. All the activated pixels are set in the 374-th column as the worst-case situation. The expected results were successfully acquired up to 432-MHz operation. The image sensor attains a frame access rate of 394.5 kHz, which corresponds to 1052 range maps/s

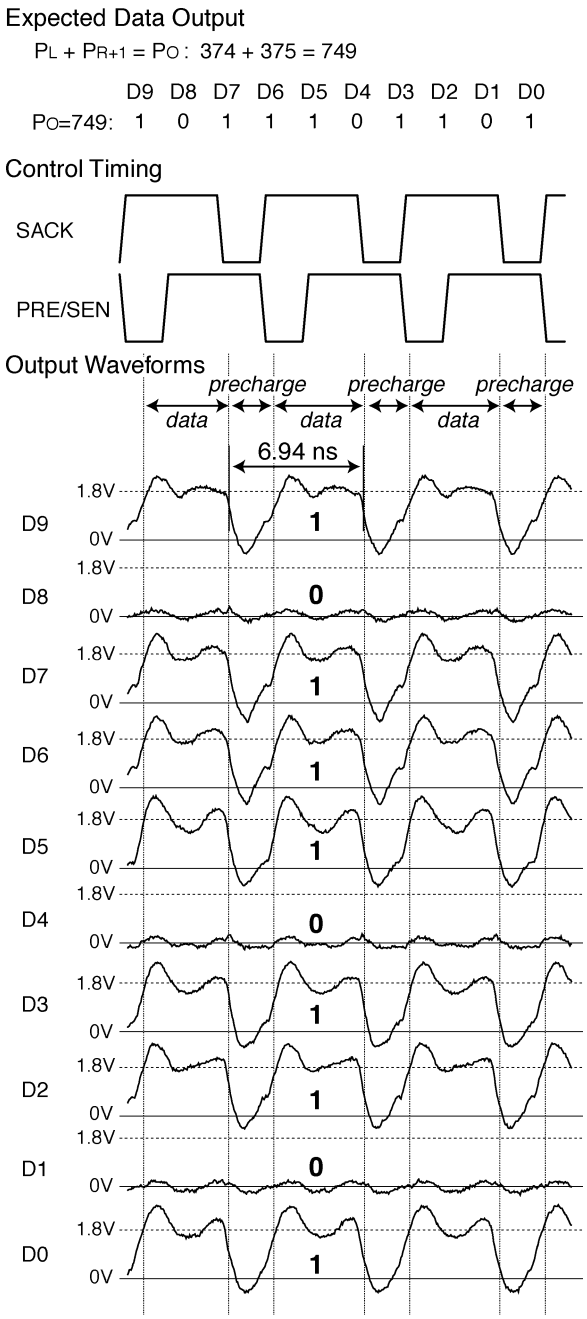

Fig. 18. Measured waveforms of the worst-case frame access to electrical test pattern at 432 MHz.

with 375 × 365 range data. The data rate is 144 Mbit/pin·s in the maximum frame access rate.

B. Range Accuracy

Fig. 20 shows the measured range accuracy at a target distance of around 600 mm. The *X* axis represents target distance and the *Y* axis represents measured distance. Fig. 20(a) shows the measured results in the conventional single sampling mode. The maximum range error is 2.78 mm and the standard deviation of error is 1.02 mm. The conventional single sampling mode achieves 0.46% range accuracy with 0.5 sub-pixel resolution. The range error is typically dominated by the pixel quantization error of position detection on the focal plane. Therefore, the

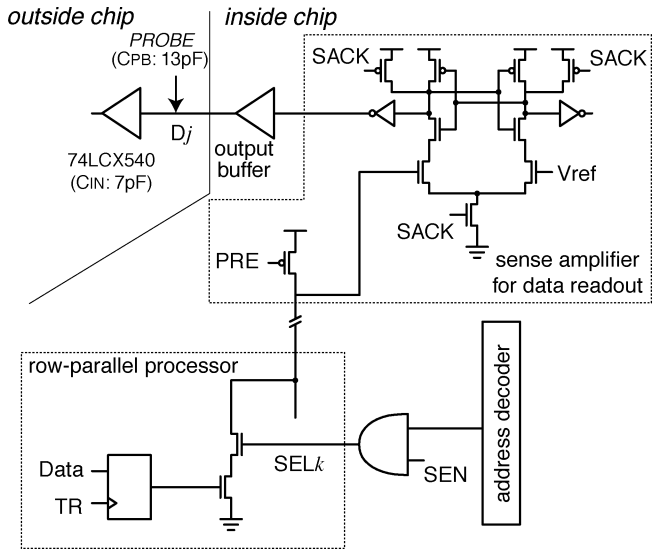

Fig. 19. Test equipment for the worst-case frame access.

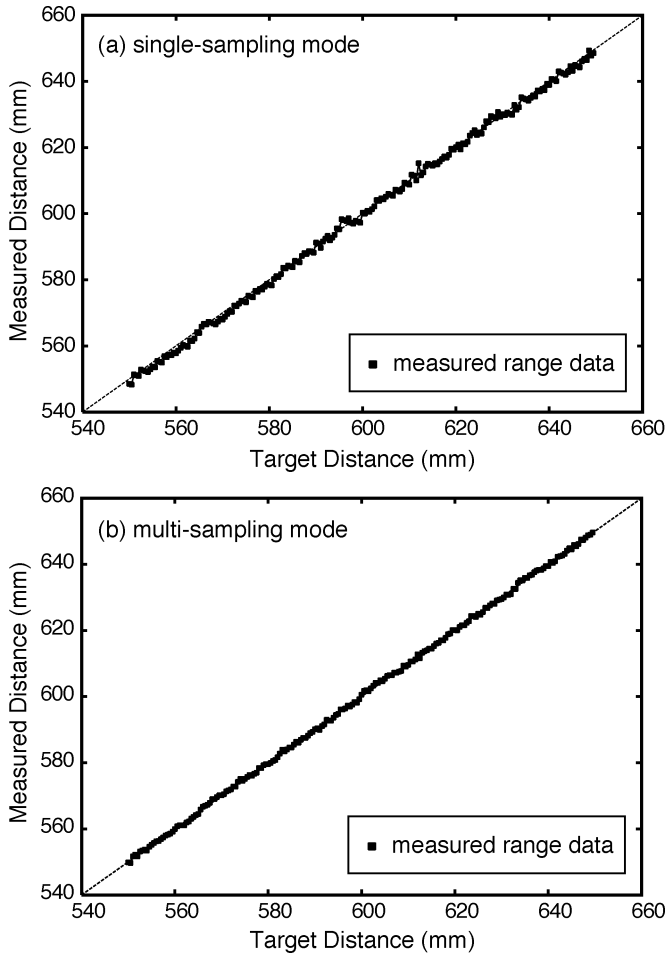

Fig. 20. Measured range accuracy. (a) Single-sampling mode. (b) Multisampling mode.

range error can be suppressed by the multisampling technique with four scales as shown in Fig. 20(b). The maximum range error is 1.10 mm and the standard deviation is 0.47 mm in the same situation. The multisampling mode attains 0.18% range accuracy, which corresponds to around 0.2 sub-pixel resolution.

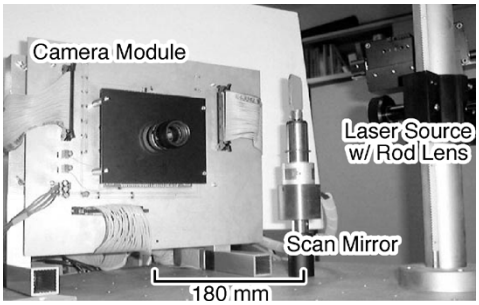

Fig. 21. Photograph of a range finding system.

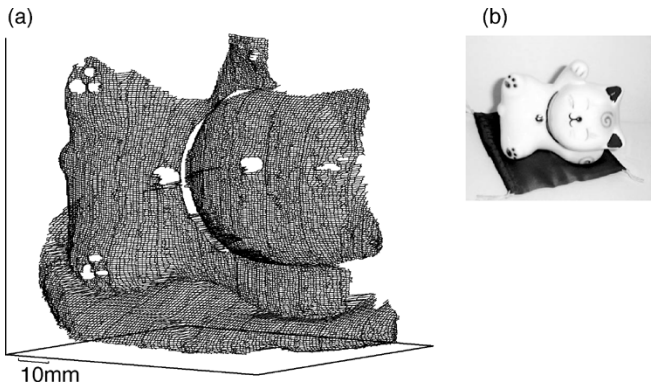

Fig. 22. Measurement result of range finding. (a) Measured range data. (b) Target object.

The range accuracy suffers from fluctuation of the threshold voltage of pixel activation. The peak-to-peak threshold fluctuation is about 150 mV including the reset voltage drop on the sensor, which is calculated by binary 2-D images that are measured using various reset voltages. However, the intensity profile with four scales does not fatally suffer from the fluctuation because the fluctuation has strong correlation with the location on the sensor and it is small enough to still allow the calculation of the center position in a local area. The timing of pixel activation is separated from the search and address acquisition operations as shown in Fig. 8. That is, the pixel activation is executed after the search path refresh and before the search signal propagation. Therefore, the pixel activation is not affected by crosstalk caused by digital signaling on the focal plane.

C. Example of Measured Range Image

Fig. 21 shows a photograph of the present measurement setup. The baseline between a camera and a beam projector is set to 180 mm. The target distance is 600 mm and the target scene is 90×90 mm^2. A 300-mW laser beam is expanded by a rod lens as a sheet beam with 5 mm width. The beam wavelength is 635 nm. Fig. 22 shows an example of measured range images. The measured 3-D data are plotted on three-dimensional coordinates as a wire-frame model (a) of a target object (b) in Fig. 22. In the present measurement setup, the limiting factor of the range finding is the pixel activation time. So the system requires a higher sensitivity photo detector or a sharp and strong laser beam. Our future work is to get better performance of the designed image sensor by satisfying these system requirements. Table II summarizes the chip performances.

TABLE II
CHIP PERFORMANCE

Supply voltage	1.8 V
Max. clock freq.	432 MHz
Frame access rate	394.5 kHz
Data rate	144 M bit/pin/sec
Range finding speed	1052 range maps/sec
Sub-pixel resolution	0.2 pixels (4 samplings)
Range accuracy	max. 1.10 mm @ 600 mm
	S.D. 0.47 mm @ 600 mm
Power dissipation	1065 mW @ 432 MHz, 1.8 V

VII. CONCLUSION

We have presented a high-speed 3-D image sensor for a 1000 range maps/s 3-D measurement system which has many potential applications such as shape measurement of structural deformation and destruction, quick inspection of industrial components, observation of high-speed moving objects, and fast visual feedback systems in robot vision. A row-parallel frame access architecture has been proposed for the high-speed range finding. The row-parallel search operations are executed by a chained search circuit embedded in a pixel on the focal plane. The bit-streamed column address flow enables row-parallel address acquisition with a compact circuit implementation. Moreover a multisampling technique is available for range accuracy improvement. A 375×365 3-D range-finding image sensor has been designed and fabricated in a one-poly five-metal (1P5M) 0.18-μm standard CMOS process. It attains a high-speed frame access rate with multiple samplings. The maximum frame access rate is 394.5 kHz with four samplings, which has a potential capability of 1052 range maps/s in the case of a sufficiently strong beam intensity. Then it provides 1.10 mm range accuracy at a target distance of 600 mm. It has been improved up to 0.2 sub-pixel resolution by the multisampling technique.

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