Three Dimensional Image Sensor for Real Time Application Based on Triangulation

Kunihiro Asada[†‡], Yusuke Oike[†], and Makoto Ikeda[†‡]

[†]Dept. of Electronic Engineering, University of Tokyo
[‡]VLSI Design and Education Center (VDEC), University of Tokyo
7–3–1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
Phone: +81-3-5841-6719, Fax: +81-3-5841-8912
E-mail: {y-oike, ikeda, asada}@silicon.u-tokyo.ac.jp

Abstract

A real-time 3-D image sensor with VGA (640 × 480) resolution based on triangulation is presented. The sensor employs an adaptive thresholding circuit and column-parallel time-domain approximate ADCs to realize high-speed readout for real-time range finding. Sub-pixel position calculation based on intensity profile by the readout scheme achieves high-accuracy range finding. A column-parallel position detector suppresses redundant data transmission for a real-time measurement system. A real-time 3-D imaging system integrated with the present sensor has been developed and successfully demonstrated. Moreover a row-parallel range finding sensor is also presented for 1000 range maps/s.

Keyword: Three dimentional image sensor, real time, VGA, light-section method, triangulation

I Introduction

In recent years we often see 3-D computer graphics in movies and televisions, and handle them interactively using personal computers and video game machines. Latest and future 3-D applications require both higher pixel resolution for accurate range finding and higher frame rate for real time, not only just 3-D image. Fig.1 shows a structure of 3-D measurement system based on a light-section method. The system allows highly accurate range finding by simple triangular calculation. It, however, requires thousands of images every second for real-time 3-D measurement. For example, a 1024 × 1024 range map in video rate needs 30k fps. It is difficult for a standard readout architecture such as CCD. Even the high-speed CMOS APS using column-parallel ADCs [1] realizes 500 fps at most.

Some position sensors for the fast range finding are reported in [2]–[4]. The sensor using a row-parallel winner-take-all (WTA) circuit [2] can acquire a 64 × 64 range map in 100 range_map/sec. Its pixel size can be smaller than [3] due to the row-parallel architecture. The pixel resolution, however, is limited by the precision of the current-mode WTA circuit. It is difficult to realize enough high frame rate for real time with high pixel resolution. The sensor using pixel-parallel architecture [3] can acquire a 192 × 124 range map in video rate. It has a large circuit for frame memories and an ADC in pixel. Therefore they developed 160 × 120 3-D imager with analog frame memories out of a pixel array [4]. It makes a pixel circuit smaller and realizes high resolution as a QVGA color imager. It, however, sacrifices range finding rate and it is also difficult to get 3-D image in real time with higher pixel resolution.

In this paper, we present the first real-time 3-D image sensor with the capability of VGA (640 × 480) resolution [5], and also introduce a row-parallel range finding sensor for 1000 range maps/s [7]. We propose two techniques for high-resolution and real-time range finding: a high-speed readout scheme and a column-parallel position detector. The high-speed readout scheme using adaptive thresholding and time-domain approximate ADC achieves high frame rate for real-time range finding and high range accuracy due to sub-pixel position calculation. In addition, it allows to use a standard and compact pixel circuit for high pixel resolution. A real-time and high-resolution 3-D imaging has been successfully demonstrated using the developed 3-D image sensor [6]. Moreover we have proposed a row-parallel position detection architecture for 1k frames/s range finding. It has a future possibility of advanced applications such as observation of deformation and destruction, quick inspection of industrial components and a fast visual feedback system in robot vision.

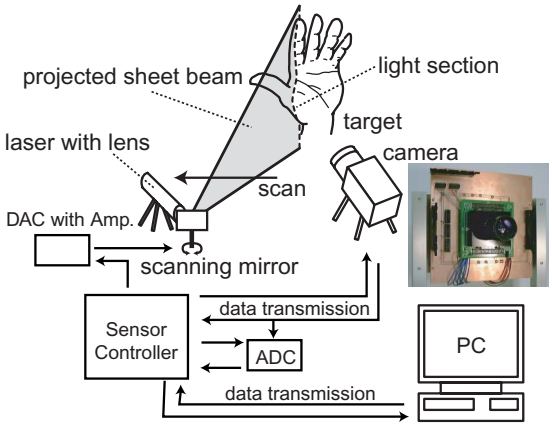

Fig. 1 3-D Measurement System Based on Light-Section Method.

II Real-Time and High-Resolution 3-D Image Sensor

Fig.2 shows the proposed sensing procedure for high-speed position detection. For 2-D imaging, all pixels are accessed using raster scan. On the other hand, a row line is accessed using the high-speed readout scheme, which is realized by adaptive thresholding and time-domain approximate ADCs (TDA-ADCs) in 3-D mode (a). Some pixels in a row line, where a strong light incidents, are detected for the location of the projected sheet beam when the pixel value is over the threshold level decided by dark pixel values adaptively (b). The pixel values over the threshold level are converted to digital by column-parallel TDA-ADC (c). The adaptive thresholding and the approximate ADC are carried out at the same time as dynamic

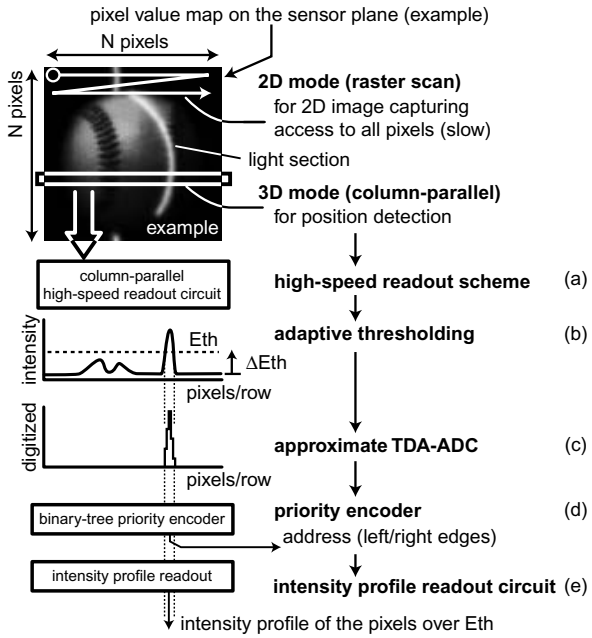

Fig. 2 Sensing Procedure for High-Speed Position Detection.

pixel value reading. The results of the adaptive thresholding are transferred to a binary-tree priority encoder (PE) to get the left and right edge addresses of the detected pixels (d). The next stage outputs the intensity profile of the detected pixels using the results of the priority decision circuit (e).

A. Circuit Configuration

High-Speed Readout Scheme

Fig.3 shows a structure of high-speed readout scheme. In the present architecture, a pixel circuit can be the same as the 3-transistor CMOS APS [1]. This pixel structure realizes a small pixel area and high pixel resolution in general. In 2-D mode, PC is set to low and SW is set to low so that pixels work as the conventional APS. In 3-D mode, SW is set to high and column lines are precharged by giving a negative pulse signal to PC. After a row line is selected, the column outputs V_{col} begin to decrease depending on each pixel value as shown in Fig.3(a). Namely V_{col2} associated with pixels of a strong incident light is decreasing more slowly and its column output CMP_2 is enabled later as shown in Fig.3(b).

Adaptive Thresholding Circuit

In general, the conventional position sensor detects the pixels of stronger intensity than the fixed threshold intensity. In our sensing scheme, the threshold intensity E_{th}, shown in Fig.2 (b), is decided adaptively by the weakest intensity in each row as shown in Fig.3 (c). The common trigger signal COM is initiated by the column output of the darkest pixel. It propagates to the first stage of column-parallel latch sense amplifiers (SAs) through a delay T_{th}. The delayed signal $DCK0$ latches the column outputs CMP in parallel, that is, it detects late-arrival column outputs. The late-arrival stands for the pixel of strong intensity. The first delay T_{th} keeps a threshold margin ΔE_{th}, shown in Fig.2 (b), from the darkest level in time domain. The results ACT of the first stage latch indicates whether a pixel is activated or not. They are transferred to the next priority encoder stage.

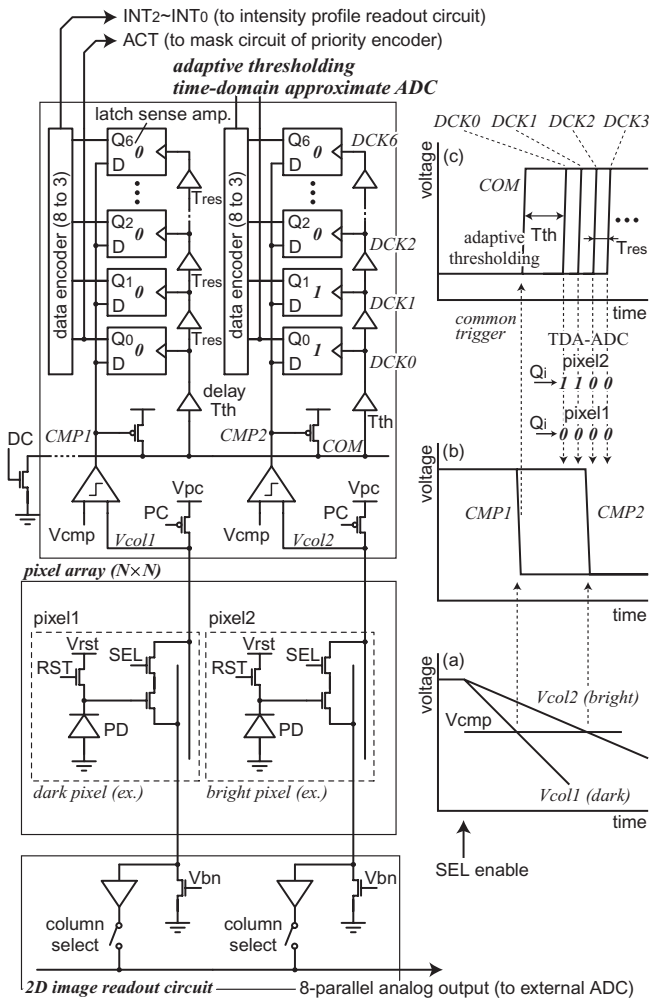

Fig. 3 Schematic and Operation of high-speed readout scheme.

Time-Domain Approximate ADC

The intensity of the activated pixels can be acquired by a column-parallel time-domain approximate ADC (TDA-ADC). The common trigger signal COM continues to propagate through a delay T_{res} as SA clock signals DCK_n as shown in Fig.3(c). DCK_n latches the column outputs CMP at the n-th stage one after another as shown in Fig.3(b). The arrival timing of a column output depends on the pixel value, so the results INT_2–INT_0 of TDA-ADC show an approximate intensity of each selected pixel normalized by the darkest pixel in the row.

Column-Parallel Position Detector

Adaptive threshold results ACT are received by a binary-tree priority encoder (PE). It consists of a mask circuit, a binary-tree priority decision circuit and an address encoder. At the mask circuit, ACT_n is compared with the neighbors ACT_{n+1} and ACT_{n-1} to detect the left and right edges. The priority decision circuit receives input signals from the mask circuits and generates the output at the minimum address of activated pixels. The addresses of the left and right edges are encoded at the address encoder. After the first-priority edge has been detected, the edge is masked in accordance with the outputs of priority decision. And then the location of the next priority of activated pixels is encoded. Our improved priority decision circuit keeps high speed in large input number due to a binary-tree structure and a compact circuit cell. Its delay increases in

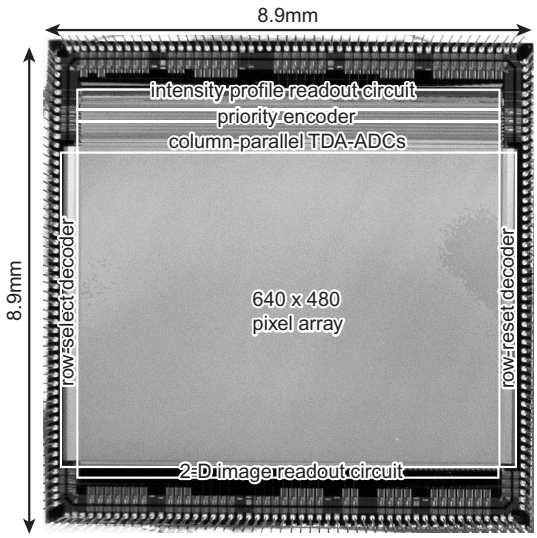

Fig. 4 Chip Microphotograph.

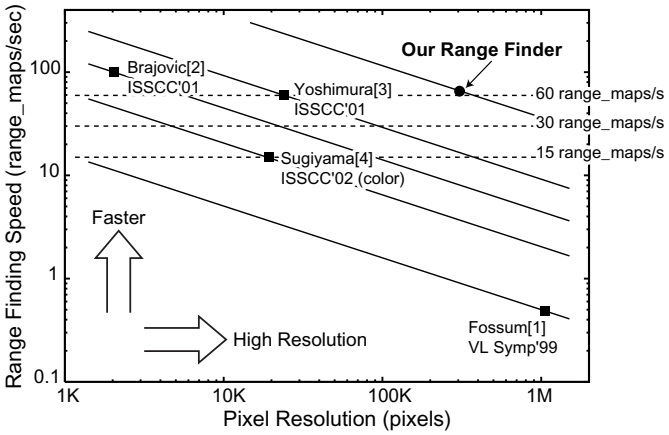

Fig. 5 Range Finding Speed and Pixel Resolution.

proportion to $\log(N)$, where N is input number.

B. Chip Implementation of VGA 3-D Image Sensor

We have designed and fabricated a 640 × 480 range finder using the present architecture and circuit in 0.6 μm CMOS process. Fig.4 shows its chip microphotograph and components. The sensor has a 640 × 480 pixel array, row select and reset decoders, 2-D image readout circuit, column-parallel TDA-ADCs, a 640-input priority encoder and an intensity profile readout circuit in 8.9 mm × 8.9 mm die size. The pixel has a photo diode and 3 transistors. Its area is 12 μm × 12 μm with 29.5% fill factor.

C. Measurement Results of Real-Time 3-D Imaging

The fabricated range finder has been mounted on a test board in 3-D measurement system based on a light-section method as shown in Fig.1. The 3-D measurement system is composed of the camera, a laser (wavelength 665 nm) with a rod lens for beam extension, a scanning mirror with a DAC, an ADC for 2-D imaging, an FPGA for sensor control, and a PC for display.

Frame Rate

In 2-D imaging, 8 pixel values are readout in parallel and it takes 2 μs. The maximum 2-D imaging speed is 13 fps (frames/sec) using 8-parallel high-speed external ADCs. It has a potential of higher speed of 2-D imaging since it is easy to implement the conventional readout techniques for 2-D imaging in our sensor architecture.

In 3-D imaging, the precharge voltage V_{pc} is set to 3.5 V and the compared voltage V_{cmp} is set to 3.0 V. Activated pixels in a row line are accessed and detected in 50 ns. The delay time of the priority encoder stage is 17.2 ns for the left and right edges. The readout time of the intensity profile is 21.5 ns. Their stages are pipelined. Therefore the location of the projected sheet beam is acquired in 24.0 μs. The range finder realizes 65.1 range_maps/sec in VGA pixel resolution. Fig.5 shows the pixel resolution and 3-D imaging speed of our present range finder with a comparison among the previous designs.

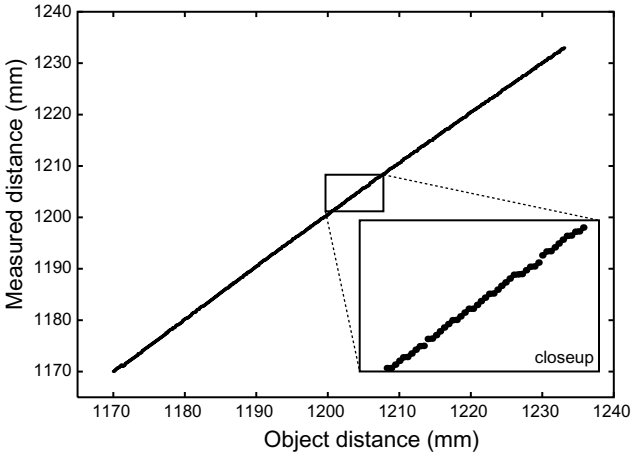

Fig. 6 Measured Range Accuracy.

Table 1 Specifications of the Real-Time 3-D Image Sensor.

Process	2P3M 0.6 μm CMOS
Die size	8.9 mm × 8.9 mm
# of pixels	640 × 480 pixels (VGA)
# of transistors	1.12M transistors
Pixel size	12.0 μm × 12.0 μm
# of trans. / pixel	3 transistors
Fill factor	29.54 %
Power supply voltage	5.0 V
Power dissipation	305 mW (at 10 MHz operation)
Max. 2-D imaging rate	†13.0 frames/sec
Max. position detection rate	41.7k lines/sec
Max. range finding rate	65.1 range_maps/sec
Range accuracy (max. error)	0.87 mm at a distance of 1200 mm

†limited by off-chip ADC

Range Accuracy

Fig.6 shows measured distances of a white flat board by the present range finder. The standard deviation of measured error is 0.26 mm and the maximum error is 0.87 mm at a distance of 1170 mm – 1230 mm by gravity center calculation using an acquired intensity profile. For comparison, the standard deviation of measured error is 0.54 mm and the maximum error is 2.13 mm by the conventional binary-based position calculation. An intensity profile could be distorted by device fluctuation, but the measurement results show that the present range finder achieves higher accuracy than the conventional position sensor using a binary image. Table 1 shows the specifications of the present real-time 3-D image sensor.

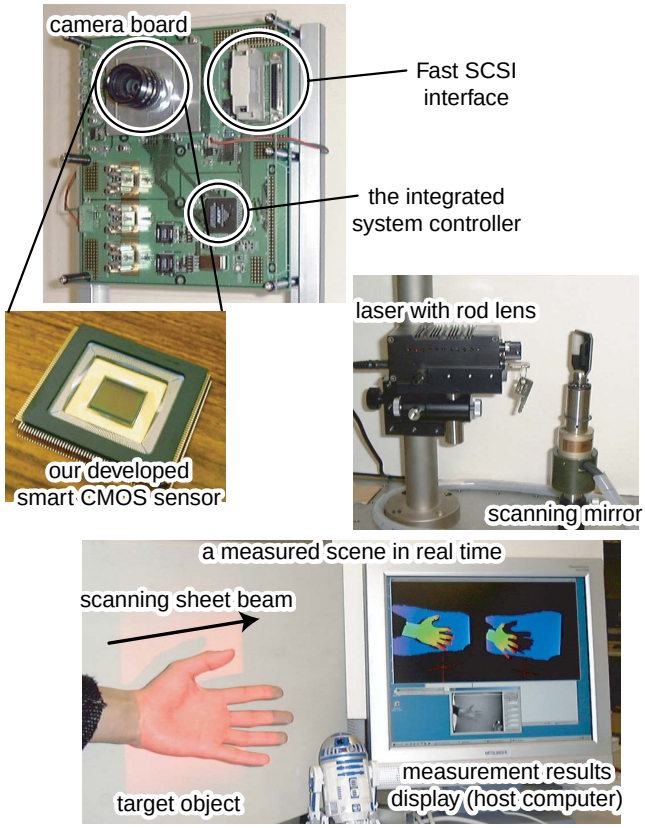

Fig. 7 Photographs of Real-Time 3-D Imaging System.

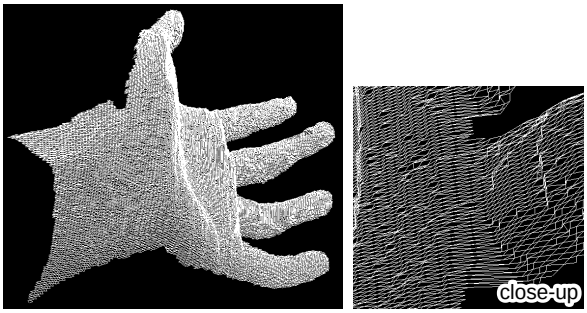

Fig. 8 Measured Range Data.

Real-Time Imaging System

Fig.7 shows our system implementation. The camera board has the developed image sensor, the integrated system controller, power supply circuits, a SCSI interface, 8-bit ADCs, a 12-bit DAC for mirror control, and peripheral logic circuits. The laser beam source with a rod lens has 300 mW power and 665 nm wavelength. The measured data are transferred and displayed on a host computer in real time as shown in Fig.7.

Fig.8 shows a wire frame of measured range data. A close-up of the wire frame is also shown. A target is placed at a distance of 1200 mm from the camera. The distance between the camera and the beam scanner is 300 mm. Fig.9 shows measured 3-D images in real time. The range data are plotted as a wire frame at two view angles. Moreover the color of wire frames represents the distance from the camera by the brightness. The brighter regions are closer to the camera than the darker ones.

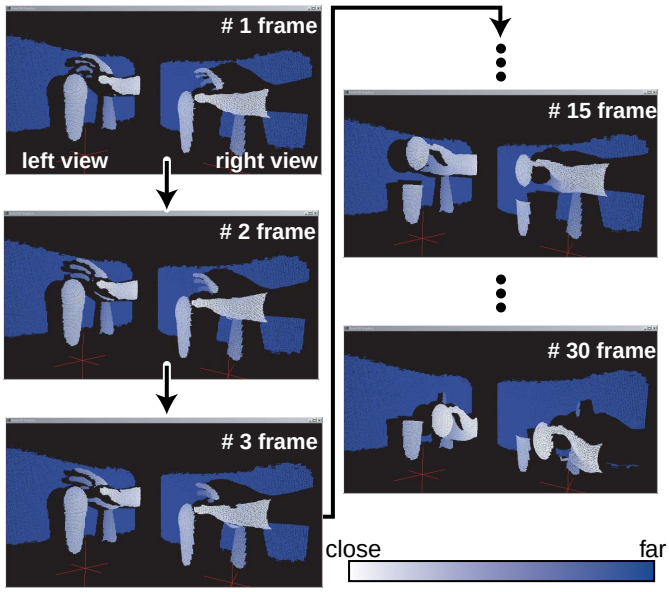

Fig. 9 Measured 3-D Images of Moving Objects.

III 1k Frames/s Row-Parallel Range-Finding Sensor

Real-time and high-resolution 3-D image sensors realize a wide variety of application fields such as gesture recognition, security systems, computer vision, movies and televisions as presented above. On the other hand, an ultra-high-speed range finding is required for future applications such as observation of deformation and destruction, quick inspection of industrial components and a fast visual feedback system in robot vision. The state-of-the-art sensors based on the light-section method [2]–[5] have been reported for real-time 3-D imaging systems of 15 fps ~ 100 fps. It is, however, difficult for them to realize ultra-high-speed 3-D measurement over 1000-fps range finding with a practical resolution. We have presented a row-parallel 3-D image sensor with 375 x 365 pixels for 1000-fps range finding based on the light-section method [7]. The row-parallel search architecture is implemented with a new multi-sampling function for a fine sub-pixel resolution using 0.18 μm standard CMOS process.

A. Row-Parallel Position Detection Architecture

Fig.10 shows a block diagram to illustrate the 3-D image sensor with the row-parallel search architecture. It consists of a pixel array, bit-streamed column address generators, row-parallel processors with 18-bit registers and output buffers, and an on-chip controller with a PLL. Additionally a row scanner and a multiplexer are used for the conventional 2-D imaging. In the row-parallel search architecture, the following ideas are employed. a) The left and right edges of consecutively activated pixels are detected alternately by a search signal propagation via chained search circuits in row parallel. It enables to detect positions of the incident sheet beam quickly regardless of the number of the activated pixels in row. b) A row-parallel acquisition of column addresses of detected pixels is realized by column-parallel address streaming. The column address streams are injected at the top of the sensor vertically and change their direction horizontally at pixels detected by the search circuits. It achieves O(log N) acquisition cycles by

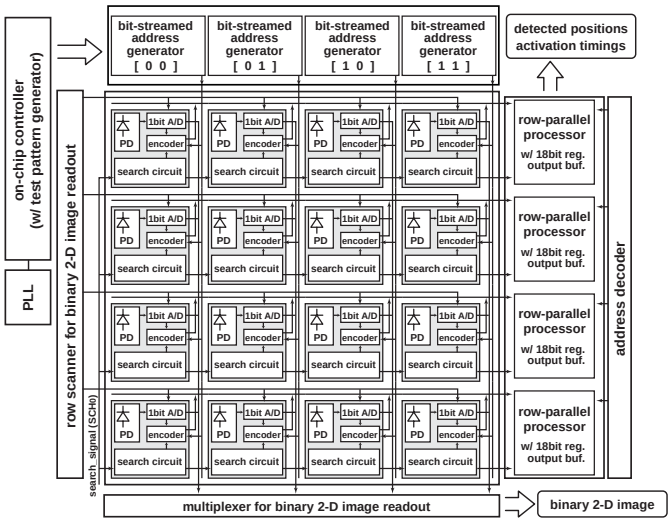

Fig. 10 Simplified block diagram of 4×4 pixels.
(The designed chip has an array of 375 × 365 pixels)

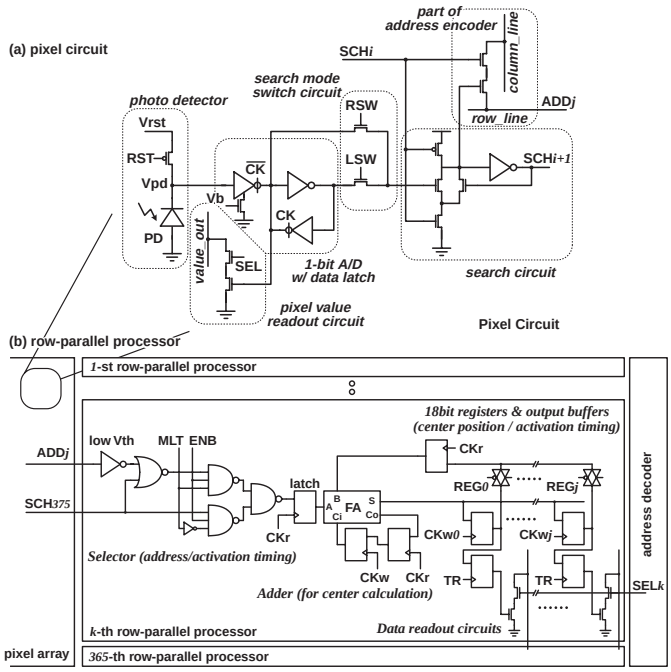

Fig. 11 Circuit configuration: (a) pixel circuit, (b) row-parallel processor.

a compact circuit of 2 FETs in each pixel in a case of a sensor with N x N pixels. c) Row-parallel processors receive the bit-streamed column address and calculate the center position of activated pixels during address acquisition. It achieves a high-speed address acquisition and a multi-sampling method. d) The multi-sampling method provides the intensity profile of incident beam to improve the sub-pixel resolution. The row-parallel processors carry out pre-processing for center position calculation to reduce the data transmission.

B. Row-Parallel Search Circuit Configuration

Fig.11 shows circuit configurations of a pixel and a row-parallel processor. Fig.12 shows their timing diagram. After photo current integration started with RST, V_{pd} is converted to digital data and latched by CK as the pixel value. Here pix-

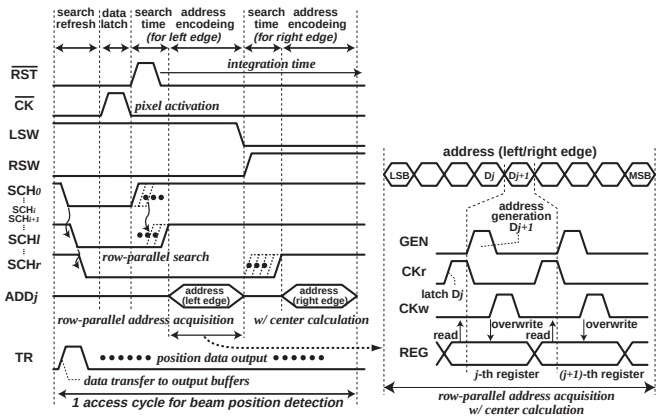

Fig. 12 Timing diagram.

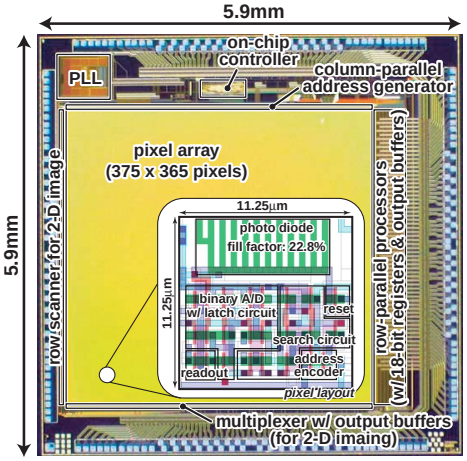

Fig. 13 Die microphotograph and pixel layout.

els with strong incident intensity are activated. V_b controls its threshold level and suppresses the short-circuit current. To detect the left edge of activated pixels, LSW is set to high and RSW is set to low. The first search trigger SCH_0 is set to low to clear the search signal propagation path (SCH_1, SCH_2, ... SCH_n). To initiate the search operation, SCH_0 is set to high in row parallel. The high level at SCH_i is transferred to the next pixel at SCH_{i+1} so far as the pixels are inactivated. Then it stops at the first-detected activated pixel (i.e. left edge) as indicated by SCH_l in Fig.12. The column address line and the row address line are connected at the detected pixel, and the bit-streamed column address ADD_j is transferred from the column line to the row line. It is received and stored by a row-parallel processor. After the address acquisition, all pixel values are inverted by LSW=0 and RSW=1. The search signal SCH_l restarts from the left edge and skips activated pixels up to the next of the right activated pixel. Then the address acquisition is carried out in the same way. The right address is added to the left address by the row-parallel processor while the address acquisition. The row-parallel processor can accumulate the detected pixel positions and count the number of samplings in order to calculate fine sub-pixel positions in post-processing. The accumulated data are transferred to output buffers by TR.

C. Chip Implementation of Row-Parallel Range Finder

The 3-D image sensor of Fig.13 has been designed and fabricated in 0.18 μm 1-poly-Si 5-metal CMOS process. It has a 375 x 365 pixel array. The pixel area is 11.25 x 11.25 μm^2 with

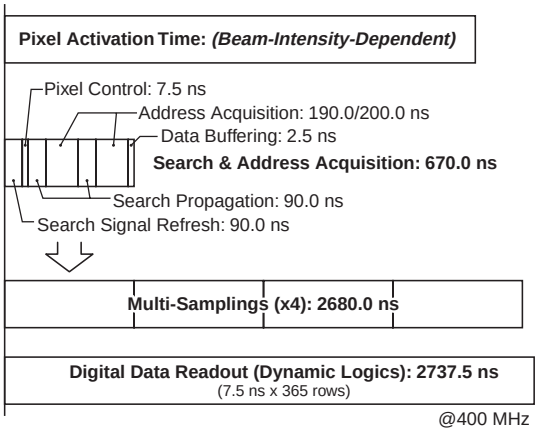

Fig. 14 Cycle times of activated pixel search and data readout.

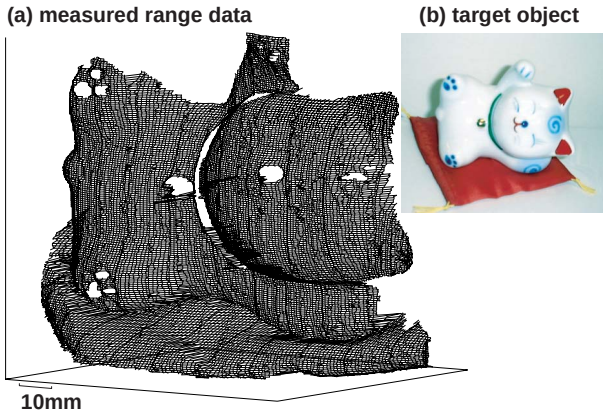

Fig. 15 Measurement result of range finding.

24 FETs and 22.8 % fill factor as shown in Fig.13. The clock signal of an on-chip controller is generated by PLL (x8/x16, 300~550MHz). The on-chip controller has a test mode to evaluate the worst-case access rate, where test image patterns are generated electrically on the sensor plane.

D. Performance Evaluation

Fig.14 shows cycle times of the activated pixel search and the data readout at a clock of 400 MHz. The pixel activation by the incident beam, the activated pixel search with the column address acquisition, and the data readout from the output buffers are carried out at the same time in a pipelined mode. The pixel activation time depends on the beam intensity and can be cut down by a sharp and strong projected sheet beam. The limiting factor of access rate is the data readout from output buffers. The multi-sampling operation can be carried out four times while the previous data readout. The worst-case test by the on-chip controller shows the maximum access rate of 394.5 kHz at 432 MHz and it corresponds to 1052 range maps/s with 375 x 365 range data. Moreover the multi-sampling method achieves 0.2 sub-pixel resolution of position detection. The measurement result shows that the maximum range error is 1.10 mm and the standard deviation of error is 0.47 mm at 600 mm distance. Fig.15 shows an example of measured range data of a target object placed at 600 mm from the sensor with a lens. The characteristics of the present sensor are summarized in Table 2.

Table 2 Specifications of the Row-Parallel Range-Finding Sensor.

Process	1P5M 0.18 μm CMOS
Die size	5.9 mm $\times$ 5.9 mm
# of pixels	375 $\times$ 365 pixels
# of transistors	3.74M transistors
Pixel size	11.25 μm $\times$ 11.25 μm
Fill factor	22.8 %
Access Rate	394.5 kHz (@ 432 MHz)
Range Finding Speed	1052 range maps/s
Range Accuracy	max. 1.10 mm @ 600 mm
Power Dissipation	1065 mW (@ 432MHz, 1.8V)

IV Conclusions

A 640 $\times$ 480 real-time 3-D image sensor using a high-speed readout scheme and a column-parallel position detector has been presented. It is the first 3-D image sensor based on a light-section method to realize VGA pixel resolution and real-time range finding. Our high-speed readout scheme realizes to use a standard and compact pixel circuit and to get the location and the intensity profile of an incident sheet beam quickly. The column-parallel position detector suppresses redundant data transmission for a real-time measurement system. The maximum range finding speed is 65.1 range_maps/sec. The maximum range error is 0.87 mm and the standard deviation of error is 0.26 mm at 1200 mm distance due to an intensity profile. In addition a row-parallel 3-D image sensor has also presented for 1k frames/s range finding. A 375 $\times$ 365 range finding sensor has been designed and fabricated in 0.18 μm CMOS process. The row-parallel position detection architecture achieves 394.5 kHz frame access rate and 0.2 sub-pixel resolution. It has the capability of 1052 range maps/s 3-D measurement. The present system provides 1.1 mm range accuracy at a target distance of 600 mm due to the multi-sampling method.

References

[1] A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E. R. Fossum, "A High Speed, 500 Frames/s, 1024 $\times$ 1024 CMOS Active Pixel Sensor," *IEEE Symp. VLSI Circuits Dig. of Tech. Papers*, 1999, pp. 137-138.

[2] V. Brajovic, K. Mori and N. Jankovic, "100 frames/s CMOS Range Image Sensor," *ISSCC Dig. of Tech. Papers*, pp. 256 – 257, 2001.

[3] S. Yoshimura, T. Sugiyama, K. Yonemoto and K. Ueda, "A 48k frame/s CMOS Image Sensor for Real-time 3-D Sensing and Motion Detection," *ISSCC Dig. of Tech. Papers*, pp. 94 – 95, 2001.

[4] T. Sugiyama, S. Yoshimura, R. Suzuki and H. Sumi, "A 1/4-inch QVGA Color Imaging and 3-D Sensing CMOS Sensor with Analog Frame Memory," *ISSCC Dig. of Tech. Papers*, pp. 434 – 435, 2002.

[5] Y. Oike, M. Ikeda and K. Asada, "640x480 Real-Time Range Finder Using High-Speed Readout Scheme and Column-Parallel Position Detector," *IEEE Symposium on VLSI Circuits Dig. of Tech. Papers*, pp.153 – 156, Jun. 2003.

[6] Y. Oike, H. Shintaku, S. Takayama, M. Ikeda and K. Asada, "Real-Time and High-Resolution 3-D Imaging System Using Light-Section Method and Smart CMOS Sensor," *in Proc. of IEEE International Conference on Sensors*, pp.502 – 507, Oct. 2003.

[7] Y. Oike, M. Ikeda and K. Asada, "A 375 x 365 3D 1k frame/s Range-Finding Image Sensor with 394.5 kHz Access Rate and 0.2 Sub-Pixel Accuracy," *IEEE International Solid-State Circuits Conference (ISSCC) Dig. of Tech. Papers*, Feb. 2004. (to be published.)