Quick Power Supply Noise Estimation Using Hierarchically Derived Transfer Functions

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ABSTRACT

The Analysis of power supply noise on VLSI chips is becoming important. In this paper we propose a new methodology for the estimation of power supply noise, caused by digital switching activity. Using transfer function calculated hierarchically from F-matrices, this method makes it possible with dramatically reduced computational cost to estimate power supply noise at all the nodes in power supply lines, which is linear to node number. The present method is shown efficient and valid enough compared with HSPICE simulation.

1. INTRODUCTION

With increasing interconnect densities and lower power supply voltage, power supply noise (or ground bounce) on VLSI chips has become an important factor for deep sub-micron design. Excessive voltage drop increases the signal delay and causes the false switching, resulting in unpredictable performance. Therefore, methods for evaluating the noise in power supply lines accurately and efficiently are needed. There are some methods to estimate power supply noise for the given input patterns [1][2]. These methods show good estimation results compared with SPICE simulation. But one of the most difficult features for estimating the power supply noise is that the voltage waveform in the power supply line is input-pattern dependent. If a circuit has n primary inputs, simulation time for the exact estimation of the maximum voltage drop is exponentially proportional to n. It is impractical to do the exhaustive simulation even if the number of primary inputs is relatively small.

Recently, a technique to find the pattern which causes the maximum voltage drop is proposed[3]. Genetic algorithm is used to find input vector pairs which cause the maximum voltage of a power feeding port of an interested block in [3]. But the input pattern may not cause the maximum voltage drop in all the nodes inside of the block. The methods proposed in [4][5][6] use Maximum Envelope Current(MEC) wave and estimate an upper bound envelope of all possible current waveforms. In [4], the estimated maximum current can be very loose upper bound because all signal correlations are ignored. In [5][6], the constraint graph is introduced to take into account the pair-wise correlations. But the estimated maximum voltage can be still too pessimistic because all possible correlations are not accounted. Even if they can be accounted, the gates may not switch in an exact timing which is given in advance. Moreover MEC is assumed to cause the maximum voltage drop in [4][5][6]. In this assumption, inductive ΔI noise effect is ignored. Though the effect of inductance in power supply lines can be ignored in low frequency, not only inductance on the package but also that of the power supply line on VLSI chips can not be ignored in deep sub-micron design [7]. It is too optimistic to estimate only IR drop in the near future. In [8], the method for estimating maximum voltage drop considering ΔI noise are proposed. But this method is pessimistic because capacitors in the power supply line are ignored.

In this paper, we do not estimate an actual noise waveform but focus on power spectral density of power supply noise and expected value of the noise waveform. To reduce computational cost, we hierarchically calculate transfer function by multiplying and transforming F-matrices which are derived by dividing power supply lines.

The rest of this paper is organized as follows. In Section 2, we propose a new technique for estimating power supply noise with reduced computational cost. Experimental results of our technique are shown in Section 3. Section 4 concludes the paper.

2. METHODOLOGY FOR EVALUATING POWER SUPPLY NOISE

2.1. Noise Calculation Using Transfer Function

Switching current in digital circuits has a complex waveform. To estimate the noise quickly, switching current is approximated as triangle waveform[7]. The

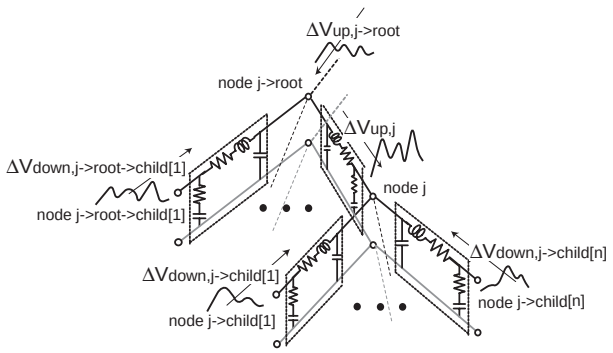

Fig. 1. Fundamental matrices in a tree structure

triangle waveform is decided by the output capacitance, gate length and gate width, etc.

In this work, we assume a multi-Pad tree or single-Pad tree design for the power network. Computational cost for estimating power supply noise is dramatically reduced by using transfer function hierarchically calculated from F-matrices tree. Even if a circuit is not composed as a complete tree structure, transfer function can be calculated by transforming F-matrix into Y-matrix .

We divide the power supply line into F-matrix blocks as shown in Fig. 1. Power line network is extracted from layout directly. An arbitrary transfer function can be calculated by multiplying and transforming F-matrices. By using transfer function which is given by calculating F-matrices, we do not need to calculate a large-scale matrix as used in HSPICE, the cost of which is generally expensive. According to [10], LU decomposition is $O(n^3)$ for an arbitrary circuit matrix. Sparse matrix packages can be used to speed up the LU decomposition to $O(n^{1.4-1.7})$ for typical matrices. On the other hand, we can estimate power supply noise at all nodes in $O(n)$ by using our method.

We define $\Delta V_j(\omega)$ as the voltage bounce at node j caused by the switching current at node j, and $\Delta V_{down,j}(\omega)$ as the voltage bounce at node j which takes into account the voltage bounce which is transferred from j's children's node as well. $\Delta V_{down,j}(\omega)$ is given as follows.

$$\begin{aligned} & \Delta V_{down,j}(\omega) \\ = & \sum_k H_{j->child[k]\rightarrow j}(\omega)\Delta V_{down,j->child[k]}(\omega) \\ + & \Delta V_j(\omega) \end{aligned} \quad (1)$$

where, $H_{a\rightarrow b}$ stands for a transfer function from node a to node b.[1] By scanning from each leaf of the tree to the root and from the root to each leaf of the tree, conductance to the ground at each node is calculated. Then $\Delta V_j(\omega)$ is calculated from the node conductance and node current $\Delta I_j(\omega)$. The node current, here, is a summation of currents from the connecting nodes into the node j. Transfer function $H_{j->child[k]\rightarrow j}(\omega)$ is easily calculated from F-matrices.

From Eq.(1), we can calculate $\Delta V_{down,j}(\omega)$ from leaves to the root.

After that, we calculate $\Delta V_{up,j}(\omega)$ from the root to leaves.

$\Delta V_{up,j}(\omega)$ is defined as the voltage bounce which is transferred from j's parent's node.

$\Delta V_{up,j}(\omega)$ is given as follows.

$$\begin{aligned} & \Delta V_{up,j}(\omega) \\ = & \sum_k H_{j->root->child[k]\rightarrow j}(\omega) \\ & \quad \times \Delta V_{down,j->root->child[k]}(\omega) \\ + & H_{j->root\rightarrow j}(\omega)\Delta V_{up,j->root}(\omega) \\ + & H_{j->root\rightarrow j}(\omega)\Delta V_{j->root}(\omega) \end{aligned} \quad (2)$$

From Eq.(1),(2), the voltage bounce at node j transferred from all the node, $\Delta V_{sum,j}(\omega)$, is calculated.

$$\Delta V_{sum,j}(\omega) = \Delta V_{down,j}(\omega) + \Delta V_{up,j}(\omega) \quad (3)$$

It is easily shown that this method takes O(n) to calculate power supply noise at all nodes in the power supply line.

2.2. Statistical Method

Even if the computational cost for calculating power supply noise is reduced to O(n), it takes a huge time of repetitive calculation for various kinds of input vector pairs to estimate an actual noise waveform. Therefore, statistical method is used to estimate power supply noise in this paper.

When $\Delta V_{sum,j}(t)$ are observed from $t = 0$ to $t \rightarrow \infty$, $\Delta V_{sum,j}(\omega)$ is usually continuous. But most of the gates have their own delay from clock edge and almost same switching current waveform when it switches on. Therefore we approximate the expected value of the noise waveform and the power spectral density as discrete. We define $\Delta U_j(\omega)$ as the voltage bounce at node j when the noise source at node j is activated periodically caused by the switching current at node j.

From the above approximation, we define the expected value of the noise waveform as follows.

$$E[\Delta V_j(\omega)] \equiv p_j \Delta U_j(\omega) \quad (4)$$

Here, p_j stands for the cycle-based switching probability at noise source of node j.

$E[\Delta V_{down,j}(\omega)]$ and $E[\Delta V_{up,j}(\omega)]$ are given from Eq.(1), (2), (4) in the following way.

$$\begin{aligned} & E[\Delta V_{down,j}(\omega)] \\ = & \sum_k H_{j->child[k]\rightarrow j}(\omega) E[\Delta V_{down,j->child[k]}(\omega)] \end{aligned}$$

[1] In this paper symbol "− >" is used for the pointing operation as in C language, while "→" is used for the transfer relation between two nodes.

Table 1. Our method and HSPICE results for ISCAS-85 circuits

			$\Delta\overline{V}(V)$	$\Delta\overline{V^2}(V^2)$	$\Delta\overline{V}(V)$	$\Delta\overline{V^2}(V^2)$	CPU time(s)	
Circuit	vdd nodes	FETs	our method		HSPICE		our method	HSPICE
C432	112	684	4.4×10^{-3}	1.3×10^{-4}	4.5×10^{-3}	1.4×10^{-4}	0.7	18
C880	198	1210	4.9×10^{-3}	2.0×10^{-4}	4.9×10^{-3}	1.9×10^{-4}	1.3	48
C1355	307	2047	9.8×10^{-3}	6.9×10^{-4}	9.6×10^{-3}	7.3×10^{-4}	1.9	156
C7552	1003	7086	3.7×10^{-2}	6.6×10^{-3}	3.8×10^{-2}	6.9×10^{-3}	7.8	2665

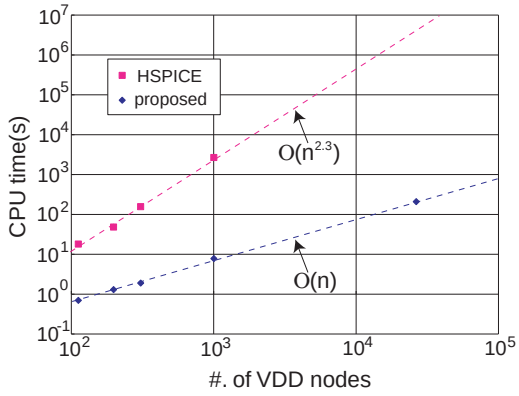

Fig. 2. Comparison between our method and HSPICE in CPU time

$$+ \quad p_j \Delta U_j(\omega) \tag{5}$$

$$\begin{aligned} & E[\Delta V_{up,j}(\omega)] \\ = & \sum_k H_{j->root->child[k]->j}(\omega) \\ & \times E[\Delta V_{down,j->root->child[k]}(\omega)] \\ + & H_{j->root->j}(\omega) E[\Delta V_{up,j->root}(\omega)] \\ + & p_{j->root} H_{j->root->j}(\omega) \Delta U_{j->root}(\omega) \end{aligned} \tag{6}$$

$E[\Delta V_{sum,j}(\omega)]$, is given as follows

$$E[\Delta V_{sum,j}(\omega)] = E[\Delta V_{down,j}(\omega)] + E[\Delta V_{up,j}(\omega)] \tag{7}$$

The power spectral density at node j is defined as follows.

$$\Delta\Phi_j(\omega) \equiv E[\Delta V_{sum,j}(\omega) \Delta V^*_{sum,j}(\omega)] \tag{8}$$

We assume that a probability of signal switching has no correlation to reduce calculation cost.

By integrating power spectral density, $\overline{\Delta V^2}$ is calculated.

3. EXPERIMENTAL RESULTS

We compare the present method with HSPICE in terms of accuracy and computational cost. Experiments are carried out on ISCAS-85 benchmark circuits implemented with 0.35μm CMOS technology. In this experiment, the standard-cell based design

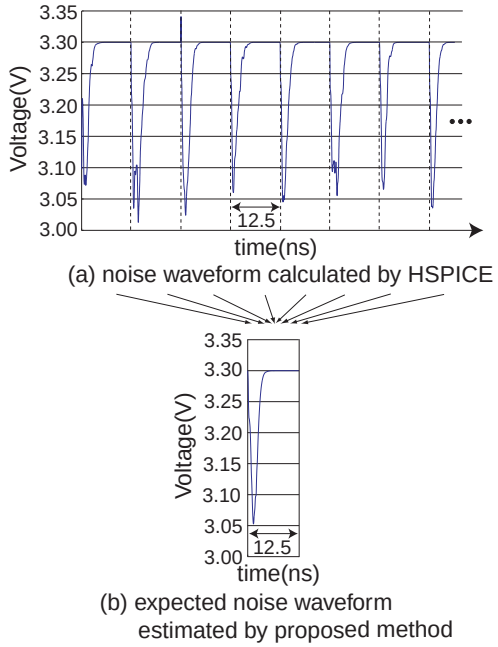

Fig. 3. Power supply noise waveform in C7552

was synthesized using Synopsys Design Compiler, and placed and routed by Avant! Apollo.[2] The switching probability of primary inputs is set to be 0.5 and the cycle of each stimulus is set to be 12.5(ns). Each gate delay and cycle-based switching probability is estimated by logic simulator beforehand.

Here we consider only off-chip inductance because the extraction of on-chip inductances is considered very difficult task. But even if on-chip inductances are considered, the present technique is available without losing accuracy and increasing computational cost by putting each inductance into F-matrix.

Table 1 shows a comparison of ISCAS-85 circuits. The values of power supply noise in Table 1 are at the most critical node in circuits. 100 input stimuli are given to calculate power supply noise in HSPICE simulation. From Table 1, we find that the error of $\overline{\Delta V}$ and $\overline{\Delta V^2}$ are within 8%.

Fig. 2 shows comparison in CPU time for ISCAS-85 circuits. Here, CPU time of HSPICE simulation is a time spent for one clock period, though the average characteristics of power supply noise simulation needs

[2]The VLSI layouts in this study are designed with Avant! CAD tools

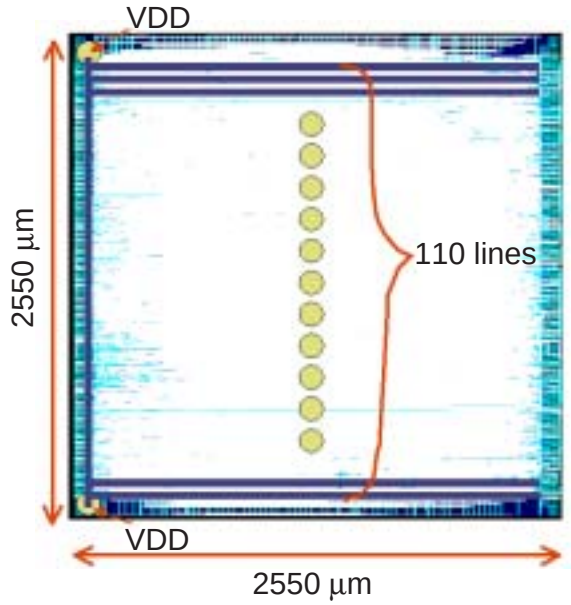

Fig. 4. layout of MCORE

huge times of repetitive simulation for various kinds of input stimuli. Computational cost in HSPICE is $O(n^{2.3})$. On the other hand, computational cost in our method is $O(n)$.

Fig. 3(a) shows a power supply noise waveform for C7552 analyzed in HSPICE and Fig. 3(b) shows an expected noise waveform estimated in our method. The expected noise waveform shows valid from Fig. 3.

We also estimate power supply noise in MCORE[3]. The number of transistors is about 200 thousand and the number of VDD nodes is about 26 thousand. The Outline of MCORE is shown in Fig. 4. Our present method requires 209 seconds. Fig. 5 shows noise map estimated by our method. Here we define the voltage dropped by noise as follows.

$$\begin{aligned} V &= V_{DD} - \overline{\Delta V} - 3\sigma \\ \sigma^2 &= \overline{\Delta V^2} - \overline{\Delta V}^2 \end{aligned}$$

On the other hand, HSPICE can not analyze noise because it exceeded memory limit. If the analysis were possible, CPU time for 1 input pattern would be about 3 million seconds from Fig. 2.

4. CONCLUSION

In this paper, we proposed a new method for estimating power supply noise based on a hierarchical calculation of F-matrices in reasonable analysis time O(n). The present method was shown to reduce computational cost extremely in estimating the power supply noise at all the nodes compared with HSPICE simulation.

[3]32bit processor core of Motorola

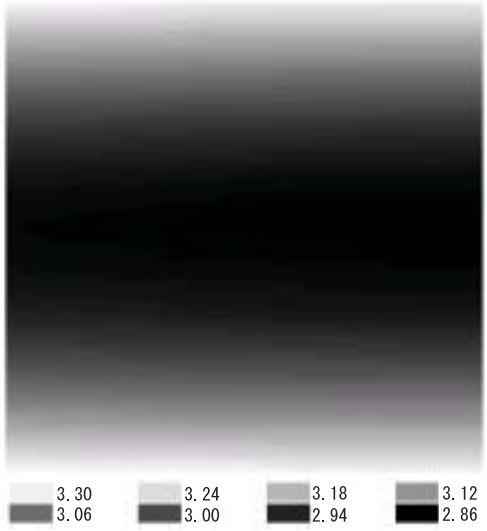

Fig. 5. noisemap of MCORE

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