A 1.8V 2.5GHz PLL using 0.18μm SOI/CMOS Technology

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SUMMARY

SOI/CMOS technology has become one of the most promising candidate for ultra high-speed devices occupied so far by GaAs and/or Si Bipolar technologies as well as a candidate for low-power and yet high-speed devices [1, 2]. Those ultra high-speed applications require phase-locked-loop (PLL) circuits for their indispensable hard-wired IPs [3] because precise clock control is critical for the circuit operation beyond GHz frequencies. Taking advantage of more than 1.35x performance gain of SOI over bulk silicon [3], SOI/CMOS devices with the help of SOI specific circuit technique will play an important role in the coming century of ultra high-speed communications.

This paper shows a 2.5GHz PLL circuit for a high-speed communication devices using a 0.18μm SOI/CMOS technology. The technology uses a shallow trench structure to effectively isolate active devices on a thin film SOI substrate. We employed floating-body SOI/CMOS in this chip. We applied a ring oscillator for the voltage-controlled-oscillator (VCO). The well-known issues of SOI would not affect circuit stability and noise performance of our PLL circuit due to the following reasons. First, as the frequency range required for VCO is comparatively narrow, the floating-body configuration would have little effect on the circuit operation [1]. Second, the thermal equilibrium on the ring oscillator can be achieved within a few micro seconds [4]. Then the self-heating issue would be insignificant for the lock-in process of the PLL. Besides, the buried oxide of SOI and shallow trench isolation reduces the cross talk noise from the large digital logic block which is the potential serious problem for system-level integration of sensitive circuits and large logic blocks.

Figure 1 shows the operating frequency of the ring oscillators. The SOI's ring oscillator is 20% faster than the bulk's under the same bias condition. This result indicates the smaller drain parasitic capacitance leads to higher operating frequency of the ring oscillator.

Figure 2 illustrates the schematic diagram of our VCO. In order to achieve the high-speed oscillation, we implemented the resistor in addition to the gate-controlled transistor in the current source of the VCO. The additional resistor reduces the output impedance of the current source transistor, and it reduces the degradation of the switch transistor. Figure 3 is the measurement result of the VCO. The VCO operates from 2.2GHz to 2.6GHz at 1.8V supply, and the VCO gain is 0.55GHz/V.

Figure 4 shows the temperature dependence of the PLL. The lower limit of the supply voltage increases as the temperature goes up. This voltage range is 1.7V to 2.1V when the PLL operates at 2.5GHz and the temperature varies from 0C to 90C. This dependence is mainly due to the characteristic of the current source resistor. In our device, the temperature coefficient of the silicided poly-Si resistor is about 0.4%/C, and it leads to the VCO frequency deviation of 20% from 0C to 90C. This frequency degradation narrows the lower margin of the supply voltage. To improve this frequency deviation, we are going to apply non-silicided poly-Si to resistor material. Then the temperature coefficient gets smaller to 1/10 and the frequency deviation of the VCO would reduce to 2% from 0C to 90C.

Figure 5 shows the waveform of the output clock. The reference clock is 156MHz and the PLL generates the 2.5GHz output clock which is the 16-times higher than the input clock.

Table 1 is the measurement result of the characteristic of the peak-to-peak (pk-pk) and root-mean-square (rms) clock jitter. HP71501B is used in this measurement to check the PLL performance to meet the international standard of the ITU-T G.813 and G.958 recommendation. The rms jitter from 12kHz to 20MHz amounts to 8.0mUI. This value is within the limit of the rms jitter of the ITU-T recommendations which is 10mUI to the output clock cycle. The pk-pk jitters are also within the limit of the recommendations (100mUI).

Figure 6 shows the jitter transfer diagram. The cutoff frequency of the jitter transfer is about 1.1MHz at 2.0V supply and 50C. This value is also within the upper limit of the jitter cutoff frequency of the recommendations (2MHz). The jitter peak gain is about 1.0dB and it does not satisfy the ITU-T specifications (0.1dB). However, this parameter can be improved by using the off-chip capacitance in the loop filter.

Figure 7 is the photomicrograph of the PLL chip. The core size is 0.11mm^2 including the on-chip filter capacitance (400pF). Table 2 summarizes the feature and performance of the PLL chip.

We have developed a 1.8V 2.5GHz PLL using a 0.18μm floating-body SOI/CMOS technology to meet the international communication standard. However, if body-fixed transistor is required for some reason, it is comparably easy to remap this design using sophisticated body contact structure. This will become one of the key component for the future ultrahigh-speed, large-scale, yet low-power system-level LSIs.

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REFERENCES
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[3] J. Eckhardt *et al.*, *ISSCC Dig. Tech. Papers*, pp. 436-437, 1999.
[4] B. Tenbroek *et al.*, *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1037-1046, 1998.

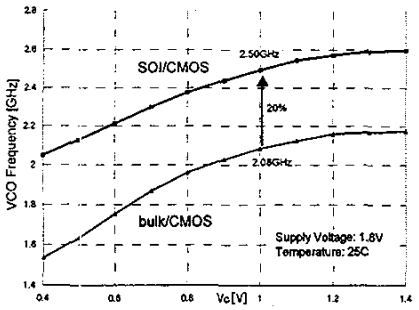

Fig. 1 VCO characteristics of SOI and bulk/CMOS by SPICE simulation

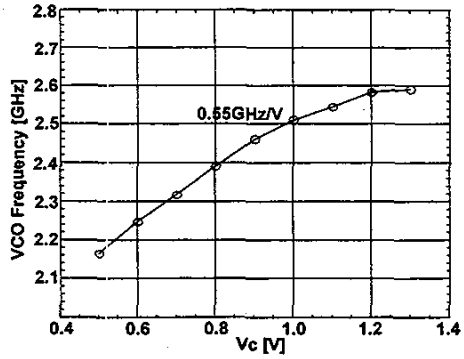

Fig. 3 Measured VCO characteristics

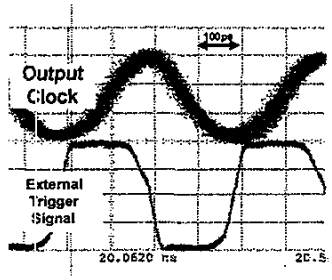

Fig. 5 Clock output waveform@2.5GHz

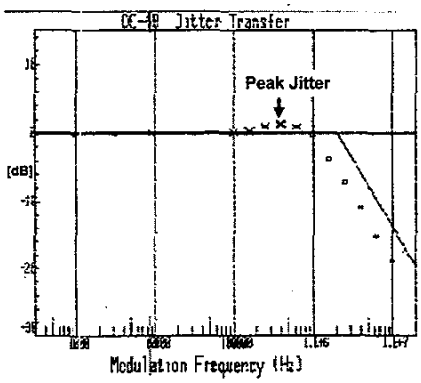

Fig. 6 Bode diagram of Jitter transfer

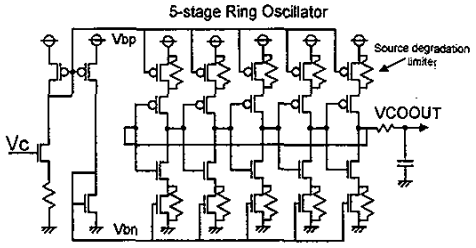

Fig. 2 Schematic Diagram of VCO

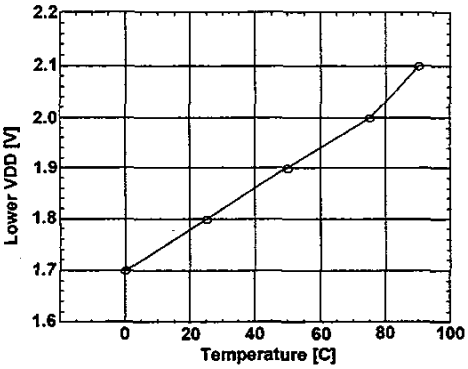

Fig. 4 Temperature dependence of PLL@2.5GHz

Table 1 Jitter generation characteristics

Operating Frequency	2.5GHz	
Supply Voltage	2.0V	
Temperature	50C	
RMS Jitter	8.0mU.I. (12kHz to 20MHz)	7.1mU.I. (1MHz to 20MHz)
Pk-Pk Jitter	47.8mU.I. (12kHz to 20MHz)	47.0mU.I. (12kHz to 20MHz)

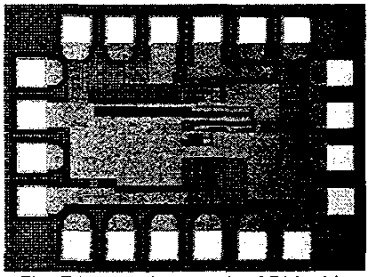

Fig. 7 Photomicrograph of PLL chip

Table 2 Features of SOI/CMOS PLL chip

Technology	0.18μm floating-body SOI/CMOS
Gate Length	0.18μm
Gate Oxide Thickness	3.5nm
Operating Frequency	2.5GHz
Supply Voltage	1.8V
Chip Size	1.15mm x 0.85mm