Power Supply di/dt Measurement using On-chip di/dt Detector Circuit

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Abstract — This paper demonstrates an on-chip di/dt detector circuit. The di/dt detector circuit consists of a spiral inductor under the power supply line which induces a di/dt proportional voltage, and an amplifier which amplifies and outputs the value. The measurement results show that the di/dt detector output and the voltage difference between a resistor have good agreement. The di/dt detector also measures the de-coupling capacitor effects for the di/dt reduction.

Introduction

As the process technology advances, the number of the transistors on a LSI chip has been increasing and their high speed operations generate more power supply noise while the low supply voltage reduces the noise margin. Thus, the power supply noise becomes a serious issue for the reliability of the LSI operations.

Recently, a di/dt noise is becoming one of the dominant source of the power supply noise along with an IR drop. An EMI noise also becomes a serious problem for high speed operating LSIs. Therefore, a current measurement technique, especially a high frequency di/dt measurement techniques, is necessary in order to estimate the di/dt noise.

Many techniques have been proposed to measure the power supply voltage bounce[1]. On the other hand, only few techniques have been developed for the power supply current measurement. One technique uses a resistor connected in series to a power supply line on a PCB board and measures the voltage difference of the both terminals using electron-beam probing[2]. This technique needs numerical calculation to obtain the current and di/dt waveforms. Another technique picks up the magnetic field and measure the spectrum[3]. It is unable to reproduce the original current nor di/dt waveforms from the spectrum because the phase information is lost.

We have proposed the basic concept of our on-chip di/dt detector circuit[4], where the simulation results showed a possibility of the di/dt detection. The focus on this paper is the experimental results of the on-chip di/dt detector circuit.

Circuit Design

A. Basic Concept

Figure 1 shows the block diagram of the di/dt detector circuit[4]. A power supply current for the internal circuit goes through the power supply line inductance L_1. A pickup inductance L_2 coupled to L_1 with a coupling coefficient K induces a di/dt proportional voltage. An amplifier amplifies the induced voltage and outputs to a 50Ω transmission line that enables a high frequency measurement. The detailed circuit with the measurement setup is shown in Fig.2.

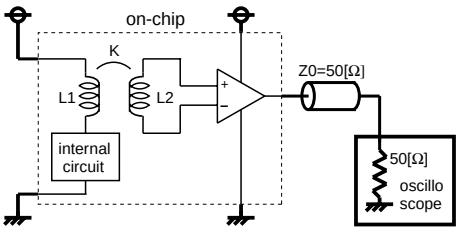

Fig. 1. Block diagram of the di/dt detector circuit.

B. Mutual Inductor

The mutual inductor consists of a spiral inductor under the power supply line. The power supply line is composed of the top metal layer, ML3, with 1 turn, 20μm width. The spiral inductor has 10 turns with 2μm width and 2μm spacing using ML1. The outside diameter of the both inductors are 140μm × 140μm. This structure is called small mutual inductor. Another type of inductors, called large mutual inductor, has 200μm diameter, and 24 turns, as shown in Fig.4. The equivalent circuit is included in Fig.2.

C. Amplifier

The amplifier schematic is also shown in Fig.2. The resistors R_b are used to keep the DC bias voltage as half-vdd where

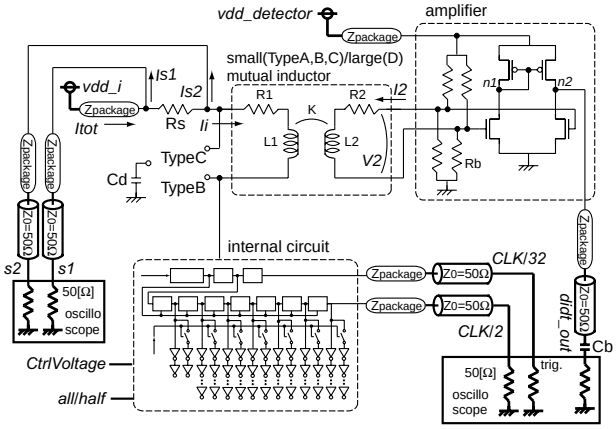

Fig. 2. Over-all circuit with the measurement setup.

the amplifier has the biggest gain. The resistance is big enough to be considered open for AC signal. The output is connected to a transmission line whose characteristic impedance is 50Ω. The blocking capacitor C_b is inserted to keep the bias voltage of node $n2$ as the same as $n1$, where the amplifier realizes the widest linearity.

Since the amplifier has complementary inputs, the common mode noise, such as the power supply bounce, is suppressed.

D. Power Supply Line Structures

The power supply line has a resistor R_s in series and the both terminals are connected to output pins, which enables the current measurement by calculating the voltage difference.

Four types of circuits were designed, as shown in Fig.2. TypeA: no de-coupling capacitor with the small mutual inductor, TypeB: the de-coupling capacitor C_d between the detector and the internal circuit with the small mutual inductor, TypeC: the de-coupling capacitor C_d between the resistor and the detector with the small mutual inductor, TypeD: no de-coupling capacitor with the large mutual inductor.

E. Internal Circuit

The internal circuit is shown in Fig.3. The *CtrlVoltage* changes the operating frequency. The 1/2 divider and 1/16 divider generate the $CLK/2$ which is the input for the DFF chain, and $CLK/32$ signal which is used as a trigger for the oscilloscope. Each DFF has an inverter chain whose switchings are the source of the di/dt. The length of the inverter chains are distributed from 2 to 12. The $all/half$ signal controls the activation ratio of the circuit.

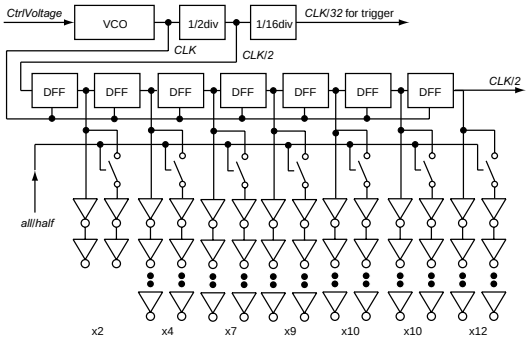

Fig. 3. Internal circuit.

F. Overview and Measurement Setup

As shown in Fig.2, the internal current goes out from *vdd_i* to the internal circuit through the package and bonding wire impedance $Z_{package}$, the series resistor R_s, and the inductor L_1. The internal circuit switching causes the di/dt which induces the voltage at the spiral inductor L_2 by the inductive coupling K. The amplifier amplifies and outputs the voltage to *didt_out*. The both terminals of the series resistor R_s are connected to the oscilloscope as the $s1$, $s2$ signals. Since the input voltage *CtrlVoltage* and $all/half$ are DC signals, no need to care the high-speed characteristics for them. The $CLK/2$ and $CLK/32$ signals come out through output buffers whose supply voltage is *vdd_io* which is neglected in the figure for simplicity. The $CLK/2$ signal is used to check if the circuit works fine, the $CLK/32$ is used as a trigger for the oscilloscope.

Analytical Model

A. Equations

The mutual inductance M is

$$M = K\sqrt{L_1 L_2}. \tag{1}$$

Assuming that the input current of the amplifier is I_2, the output voltage of the mutual inductor V_2 is

$$V_2 = M\frac{dI_i}{dt} + R_2 I_2 + L_2\frac{dI_2}{dt} \approx M\frac{dI_i}{dt} \tag{2}$$

since the input impedance of the amplifier is high and the input current I_2 is small enough to neglect the second and the third term of the equation compared with the first term.

Assuming that the gain of the amplifier is G, the output voltage of the di/dt detector circuit is

$$V_{didt\_out} = GV_2 = GK\sqrt{L_1 L_2}\frac{dI_i}{dt}. \tag{3}$$

Integrating the eqn(3) with respect to time,

$$I_i = \frac{1}{GK\sqrt{L_1 L_2}}\int V_{didt\_out}dt + C. \tag{4}$$

The relation between the internal current I_i and the voltage of $s1$, $s2$ is

$$V_{s1} - V_{s2} = R_s(I_i + I_{s2}) \tag{5}$$

and this equation can be converted to

$$V_{s1} - \left(1 + \frac{R_s}{R_t}\right)V_{s2} = R_s I_i \tag{6}$$

using $I_s = V_s/R_t$, where R_t is the termination resistance 50Ω.

From eqn(4) and (6),

$$V_{s1} - \left(1 + \frac{R_s}{R_t}\right)V_{s2} = A\int V_{didt\_out}dt + C \tag{7}$$

where

$$A \equiv \frac{R_s}{GK\sqrt{L_1 L_2}}. \tag{8}$$

Differentiate the eqn(6) by time, and with eqn(3), (8),

$$V_{didt\_out} = \frac{1}{A}\frac{d\{V_{s1} - (1 + R_s/R_t)V_{s2}\}}{dt}. \tag{9}$$

B. Parameters

According to FastHenry[5], L_1 = 0.50nH, L_2 = 14.4nH, K = 0.67 for the small mutual inductor, and L_1 = 0.86nH, L_2 = 53.3nH, K = 0.60 for the large mutual inductor, at 1GHz.

According to HSPICE simulations, the gain of the amplifier G is 0.63, the cut-off frequency is 3.8GHz if there is no load capacitance, and the output range to keep the linearity is

±0.4V. The delay of the longest inverter chain in the internal circuit is 0.625ns

The series resistor R_s is formed using gate-poly with silicide, and the designed resistance value is about 1Ω. The de-coupling capacitor C_d is formed using poly-poly capacitor, and the designed value is about 700pF. The bias resistor R_b is formed using gate-poly without silicide and the designed value is about 10kΩ.

Using these values, the designed value A of eqn(8) is $A_{design} = 0.88 \times 10^9$ in the case of the small mutual inductor.

Measurement Results

A. Process Technology

The chip was designed and fabricated using 0.35μm 2-Poly 3-ML standard CMOS technology. The chip size is 4.9mm×4.9mm and the chip photograph is shown in Fig.4.

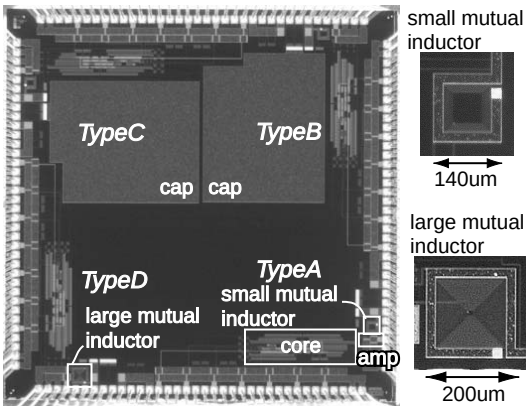

Fig. 4. Chip photograph. The chip size is 4.9mm×4.9mm.

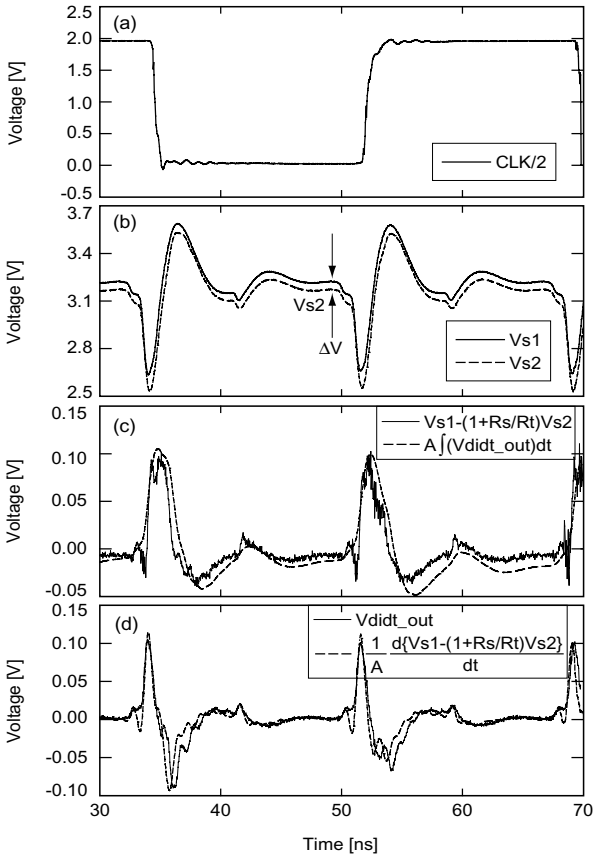

Fig. 5. Measured waveforms of (a) $CLK/2$, (b) $s1$ and $s2$, (c) $V_{s1} - (1 + R_s/R_t)V_{s2}$ signal together with the numerical-time-integral of the di/dt detector output multiplied by A, based on eqn(7), (d) the di/dt detector output with the numerical-time-differential of $V_{s1} - (1 + R_s/R_t)V_{s2}$ divided by A, based on eqn(9), of TypeA circuit.

B. Feasibility of the di/dt detector

Figure 5 shows the measured waveforms of (a) $CLK/2$, (b) $s1$ and $s2$, (c) $V_{s1} - (1 + R_s/R_t)V_{s2}$ signal together with the numerical-time-integral of the di/dt detector output multiplied by A, based on eqn(7), (d) the di/dt detector output with the numerical-time-differential of $V_{s1} - (1 + R_s/R_t)V_{s2}$ signal divided by A, based on eqn(9), of TypeA circuit. Since the $V_{s1} - (1 + R_s/R_t)V_{s2}$ waveform is noisy, we applied a smoothing before the numerical differentiation.

Here, the parameter A was fitted to match the magnitude of the waveforms, and the value is $A_{fit} = 1.2\times10^9$. The difference from A_{design} will be discussed in the following subsection.

These graphs show that the currents measured by the series resistor voltage difference and the di/dt detector output have good agreement, and our di/dt detector circuit works well.

C. The Magnitude

As we saw in the previous subsection, the magnitude has $A_{fit}/A_{design} = 1.36$ times difference between the designed and the fitted values.

The series resistance value R_s can be estimated from $s1$ and $s2$ voltage as shown in Fig.5(b). Since the internal circuit does not consume current because of no switching at the point with the arrows, the DC current going through the series resistor is the same as the current going into the termination resistor R_t of $s2$, and $I_{s2} = V_{s2}/R_t$. The series resistance value is $R_s = \Delta V/I_{s2} = R_t\Delta V/V_{s2} = 50\times(3.2225-3.1705)/3.1705 = 0.82\Omega$. However, if we assume the voltage $s2$ has 1% error, the R_s would be 1.33Ω and the A_{fit}/A_{design} would be 1.02.

In fact, we cannot distinguish which parameters, R_s, G, K, L_1 or L_2, have error from the measurement results. In general, subtraction of the similar number causes a cancellation error, such as the R_s calculation above, and the $V_{s1} - (1 + R_s/R_t)V_{s2}$ waveform. The gain of the amplifier G is also possible to have an error because of the process fluctuation.

The relative value and the shape of the di/dt is validated for now. Further TEGs measurement of the amplifier and the mutual inductor, or precise parameter extractions enhance the reliability of the di/dt detection.

D. De-coupling Capacitor Effects

Figure 6 shows the waveforms of (a) $s1$, and (b) the di/dt detector output, of TypeA, B, C circuits. The de-coupling capacitors of TypeB, C provide AC currents to the internal circuit

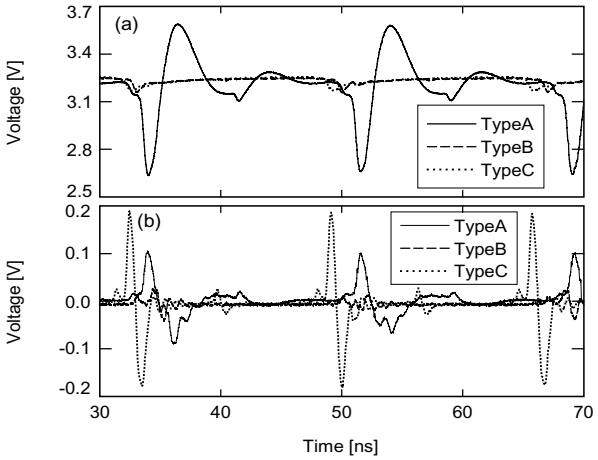

Fig. 6. Measured waveforms of (a) $s1$, and (b) the di/dt detector output, of TypeA, B, C circuits.

and few di/dt currents flow through the package parasitic inductances so that the power supply bounces are suppressed as shown in Fig.6(a).

The de-coupling capacitor on TypeB circuit suppresses the AC current going through the di/dt detector so that the di/dt detector output voltage is small, as shown in Fig.6(b). The de-coupling capacitor on TypeC circuit provides bigger and sharper AC current to the di/dt detector compared with the no de-coupling capacitor circuit of TypeA. This is because the higher impedance $Z_{package}$ of the power supply line on TypeA, while the impedance from the internal circuit to the de-coupling capacitor is smaller on TypeC circuit.

E. Activation Ratio, Mutual Inductance Dependency

The waveforms of $s1$ and the di/dt detector output voltage of TypeA, and TypeD with the large mutual inductor, and TypeA of the half activation ratio, are shown in Fig.7(a) and (b). The graph (a) shows that the power supply voltage bounce of TypeA and TypeD circuits are almost the same. This is because the same internal circuit and the same parasitics of the package $Z_{package}$, while the L_1 difference makes the small difference on the waveforms. The half activation case has the half di/dt of the internal circuit, thus the smaller voltage bounce. The voltage bounce is not half because of the parasitic capacitance of the internal circuit, the pads, the package and so on.

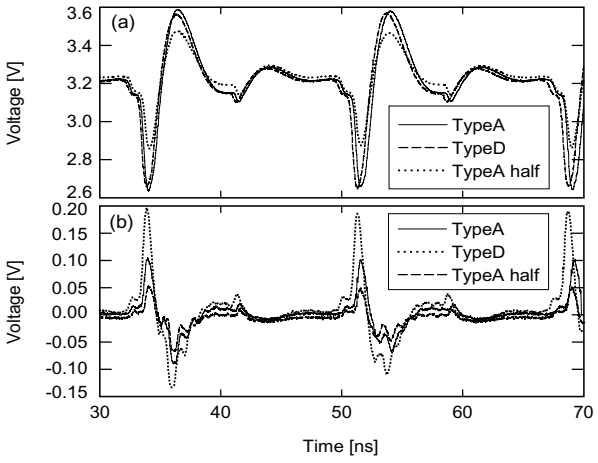

Fig. 7. Measured waveforms of (a) $s1$, and (b) the di/dt detector output voltage, of TypeA, and TypeD with the large mutual inductor, and TypeA of the half activation ratio

As for the di/dt detector output waveforms of the Fig.7(b), the waveform of TypeD circuit has almost the same shape with about 2.0 times magnitude compared with the waveform of TypeA circuit. The magnitude difference should be $K_D\sqrt{L_{1D}L_{2D}}/K_A\sqrt{L_{1A}L_{2A}} = 2.27$ if the G and the di/dt are the same, according to the eqn(3). However, the bigger L_1 of TypeD ($L_{1A} = 0.50$nH, $L_{1D} = 0.86$nH) makes smaller di/dt, resulting smaller di/dt output (2.0 times instead of 2.27 times). On the half activation ratio case, the di/dt detector output has about half magnitude with the same shape.

These results also confirm the di/dt detector performance.

Conclusion

The on-chip di/dt detector circuit has been demonstrated. Our di/dt detector circuit consists of a spiral inductor under the power supply line which induces a di/dt proportional voltage, and an amplifier which amplifies and outputs the value. The measurement results show that the di/dt detector output and the voltage difference between a resistor have good agreement. The di/dt detector also detects the de-coupling capacitor effects for the di/dt reduction. Since the on-chip and real-time di/dt measurement is possible, our di/dt detector circuit can be applicable for feedback di/dt control as well.

Acknowledgement

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