A 2.0Gbps Multiplexer and a 2.7Gbps Demultiplexer using 0.35μm SOI-CMOS Technology

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Abstract

This paper describes a 4:1 multiplexer and a 1:4 demultiplexer using 0.35μm SOI-CMOS technology for ultra high-speed telecommunication system LSIs. The multiplexer adopts a shift register architecture with a modified counter operating stably at high-frequency, while the demultiplexer adopts a 2-bit tree architecture. The multiplexer and the demultiplexer uses double-rail flip-flop circuits which can operate at high-frequency due to their reduced parasitic capacitances. The multiplexer operates at 2.0 Gbps dissipating 122 mW and the demultiplexer operates at 2.7 Gbps with 128 mW at a 2.0V supply voltage.

I. Introduction

Progresses made in LSI technologies make it possible to build system LSIs integrating high-density logics with other functions (e.g. such as analog circuits memories on a chip) offering versatile data processing as well as high-frequency and low-power operations. These system LSIs will benefit future telecommunication systems where large-scale data processing and ultra high-speed data transmission are required.

Presently, the majority of ultra high-speed multiplexers and demultiplexers developed for I/O devices in telecommunication systems are based on GaAs or Si-bipolar transistors [1]-[3]. However, GaAs devices are difficult to integrate with high-density logics. Although BiCMOS technology makes integration of high-density logics with other functions possible, it is difficult to optimize both Si-bipolar transistors and CMOS transistors for high-speed, low-voltage/power, high-reliability operations. For that reason, CMOS technology is a well-qualified technology for ultra high-speed multiplexers and demultiplexers to be used in future telecommunication systems.

Recent developments of multiplexers or demultiplexers utilize rather advanced process technologies (e.g. 0.15μm bulk-CMOS technology [4] and 0.25μm SOI-CMOS technology [5]) to achieve 3.0 Gbps operation. We focused our efforts to achieve comparable performance using the conservative 0.35μm process technology to exploit established infrastructures of circuit and technology.

In this paper, we describe a 4:1 multiplexer and a 1:4 demultiplexer for ultra high-speed telecommunication system LSIs using 0.35μm SOI-CMOS technology. The multiplexer operates at 2.0 Gbps and the demultiplexer operates at 2.7Gbps at a 2.0V supply voltage.

II. Multiplexer and Demultiplexer Design

Fig. 1 shows a block diagram of the 4:1 multiplexer using a shift register architecture. The main parts of this multiplexer are: a) the input 4-bit flip-flop circuit, b) the 4-bit shift register with selector function, and c) the 4-bit counter. We designed all of the internal circuits using complementary logic configuration to realize high-speed and stable circuit operation [5].

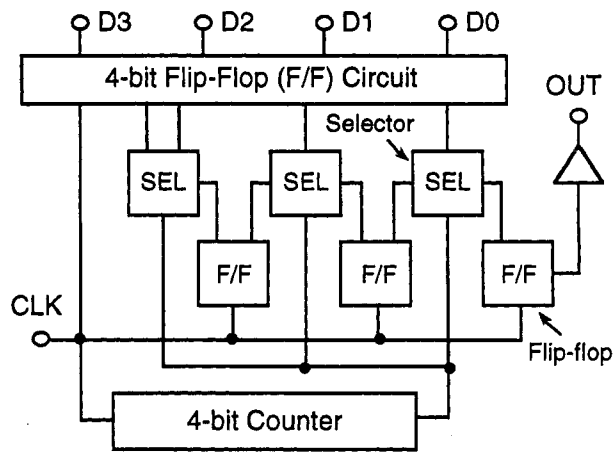


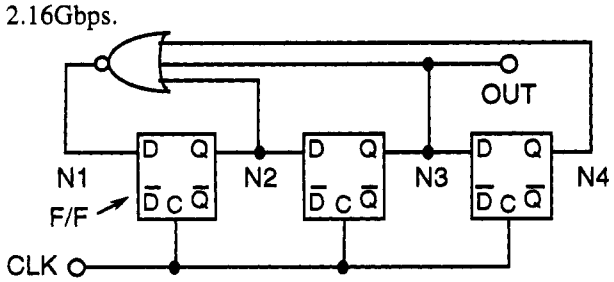
Fig. 1 Block diagram of 4:1 multiplexer.

Fig. 2 (a) shows a circuit configuration of a 4-bit counter which is often used in multiplexers and demultiplexers [3]. The 4-bit counter consists of a 3-input NOR gate and three flip-flop circuits. However, this circuit configuration sometimes leads to improper operation in the 3-input NOR gate, as shown in Fig. 2 (b). This is due to the slow output change of the flip-flop circuits, and more noticeable ones in the CMOS circuits which have weaker driving ability than in Si-bipolar circuits.

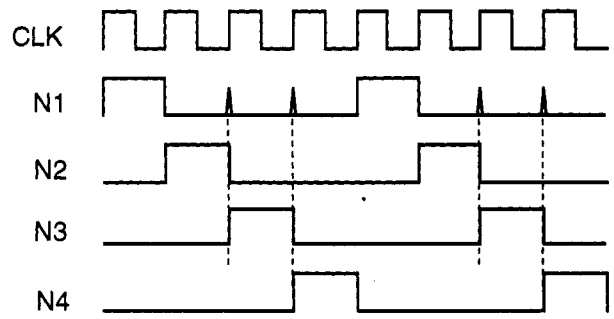
Fig. 3 (a) and (b) show the proposed circuit configuration and the timing chart of a 4-bit counter. We

connected the delay gates between the 3-input NOR gate (or 3-input NAND gate) and the flip-flop circuits to make overlapped periods of the input data of the 3-input NOR gate (or 3-input NAND gate). The 3-input NOR gate can be replaced with a 2-input NOR gate having the inputs of N4 and N5. However, in this case the output N1 of the 2-input NOR gate changes to low-level taking a long time because of the delay gates of the inverter and the 2-input NAND gates. Hence, this configuration leads to the decrease in the operating speed.

Therefore, we used the 3-input NOR gate and connected one of its input directly to the output N2 of the flip-flop circuit. From the circuit simulation using 0.35μm transistor parameters, the replacement from the 2-input NOR gate to the 3-input NOR gate increases the operating speed of the multiplexer from 1.85Gbps to 2.16Gbps.



(a) Circuit configuration

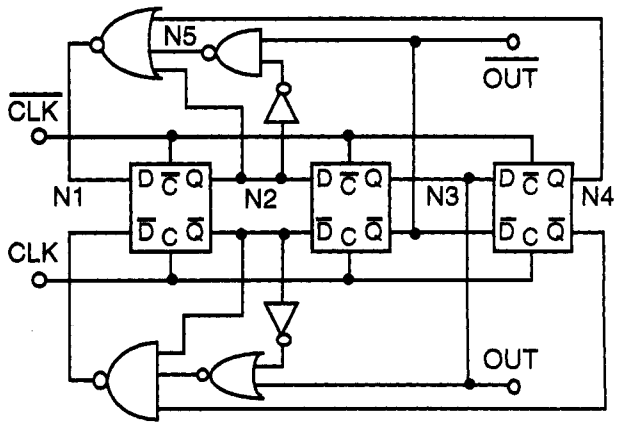


(b) Timing Chart

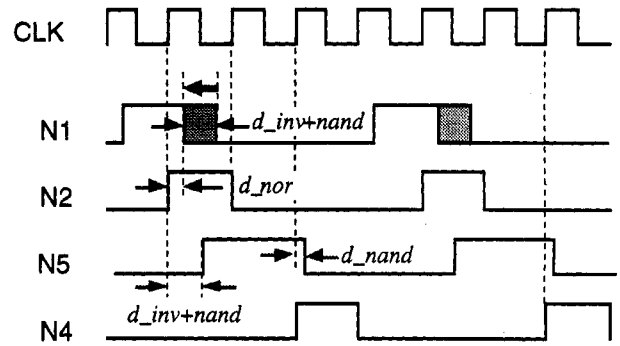
Fig. 2 Circuit operation of previous 4-bit counter.

Fig. 4 shows a block diagram of the 1:4 demultiplexer. We adopted a 2-bit tree architecture because of faster operation than other architectures [5]. The main parts of this demultiplexer are: a) the output 4-bit flip-flop circuit, b) the tree of the 2-bit demultiplexer, and c) the 4-bit divider. We also designed all of the internal circuits using complementary logic configuration for high-speed and stable circuit operation

The speed and the power dissipation of the flip-flop circuits greatly affect the performance of the multiplexers and the demultiplexers. Fig. 5 shows the double-rail type flip-flop circuit that we have already proposed [6]. The pass transistors are constructed with only NMOS transistors. The PMOS transistors, whose drains and gates are cross-coupled in the data retention loops, pull up the threshold voltage drop of the NMOS pass transistors. This flip-flop circuit can operate faster than earlier double-rail circuit due to the reduced parasitic capacitances, and adopted this flip-flop circuit to the multiplexer and the demultiplexer to attain high-speed circuit operation.



(a) Circuit configuration



(b) Timing Chart

Fig. 3 Circuit operation of proposed 4-bit counter.

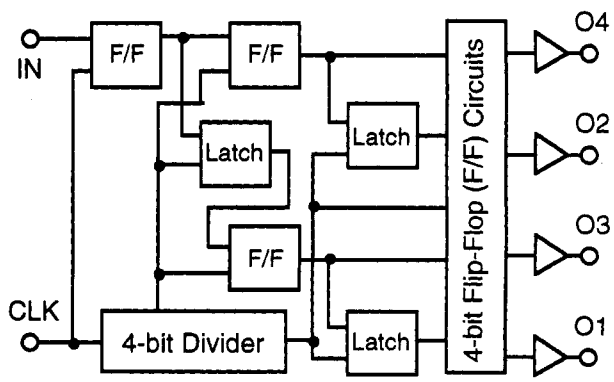


Fig. 4 Block diagram of 1:4 demultiplexer.

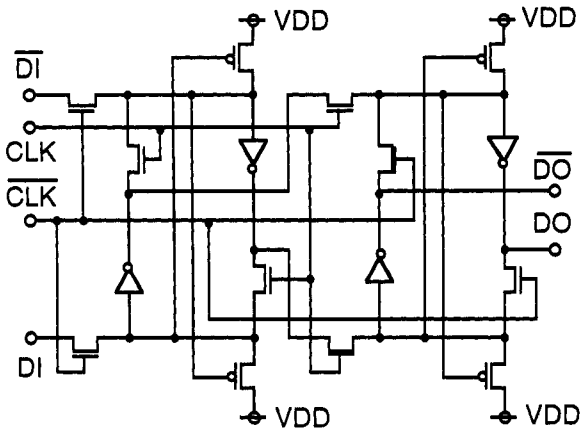


Fig. 5 Double-rail flip-flop circuit.

III. Experimental Results

We fabricated the 4:1 multiplexer and the 1:4 demultiplexer with a 0.35μm single poly-silicon and double-metal SOI-CMOS process. Fig. 6 shows a cross section schematic of the SOI-CMOS transistors. The SOI thickness is 100nm, while the buried-oxide thickness is 400nm. To lower the threshold voltages for low voltage circuit operation, we adopted the p+ poly-Si gate for the PMOS transistors and used the n+ poly-Si gate for the NMOS transistors. Table 1 summarizes the characteristics of the SOI-CMOS transistors.

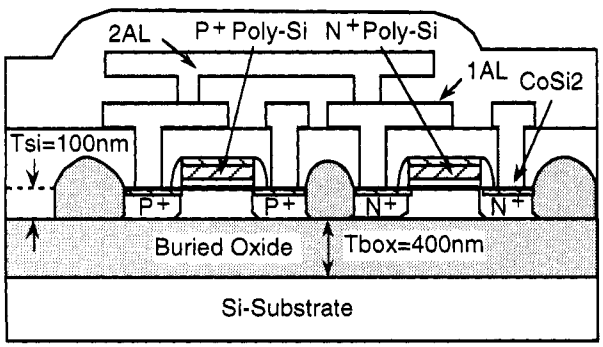


Fig. 6 Cross section of SOI-CMOS transistors.

Table 1. Characteristics of SOI-CMOS transistors.

Supply Voltage	2.0 V
Gate Length	Lgp/Lgn = 0.35μm/ 0.35μm
Gate Oxide Thickness	7.0 nm
Threshold Voltage	Vtp/Vtn = -0.33V/ 0.12V
Drain Current (W=10μm)	Idp/Ign = -0.89mA/ 3.32mA

Fig. 7 shows a photomicrograph of the multiplexer. The chip size is 1.15mm by 0.85mm, and the demultiplexer was also made using the same area size. The multiplexer and the demultiplexer were manually designed using the SOI-CMOS transistors without the body-contacts to reduce their area sizes.

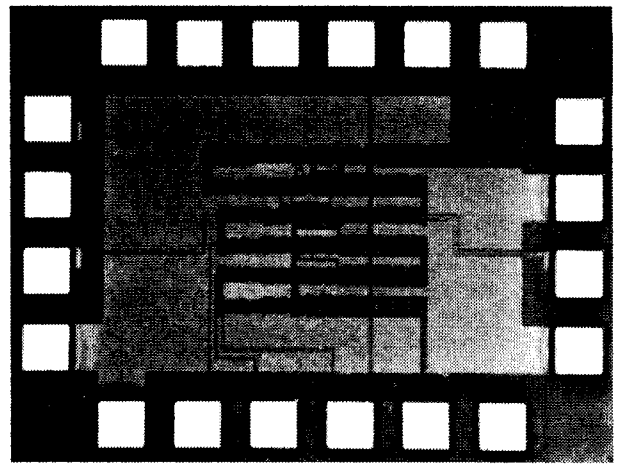


Fig. 7 Photomicrograph of 4:1 multiplexer.

Fig. 8 shows the maximum operating speed and the power dissipation of the multiplexer. The data were gathered from the packaging chips at room temperature. At a supply voltage of 2.0V, the multiplexer operated up to 2.0Gbps dissipating 122mW. Fig. 9 shows the operating waveforms of the multiplexer at the maximum data rate of 2.0Gbps. The output waveforms were observed through an external 50 ohm resistor. Parallel fixed data of 4-bits were inputted to the multiplexer.

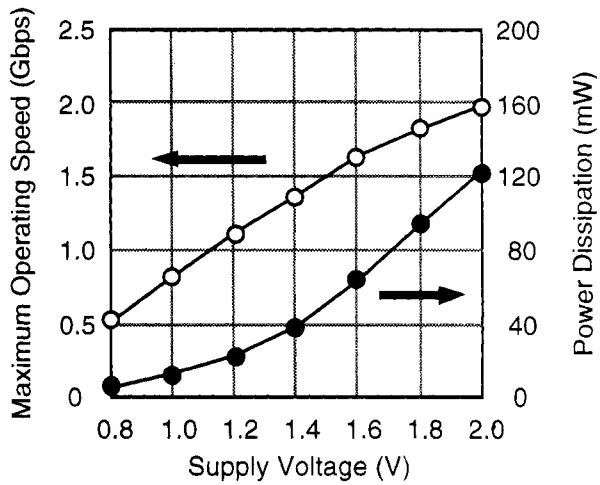


Fig. 8 Speed and Power of 4:1 multiplexer.

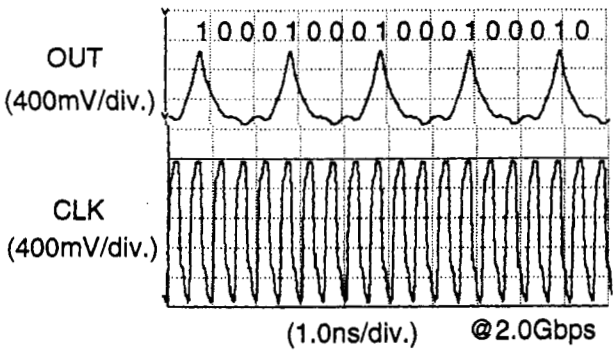


Fig. 9 Operating waveforms of 4:1 multiplexer.

Fig. 10 shows the maximum operating speed and the power dissipation of the demultiplexer. At a supply voltage of 2.0V, the multiplexer operated up to 2.7Gbps dissipating 128mW. Even at a low supply voltage of 1.0V, the demultiplexer operated up to 1.3Gbps while dissipating only 14mW. Fig. 11 shows the operating waveforms of the demultiplexer at the maximum data rate of 2.7Gbps. The serial data with a data length of 16-bits were inputted to the demultiplexer.

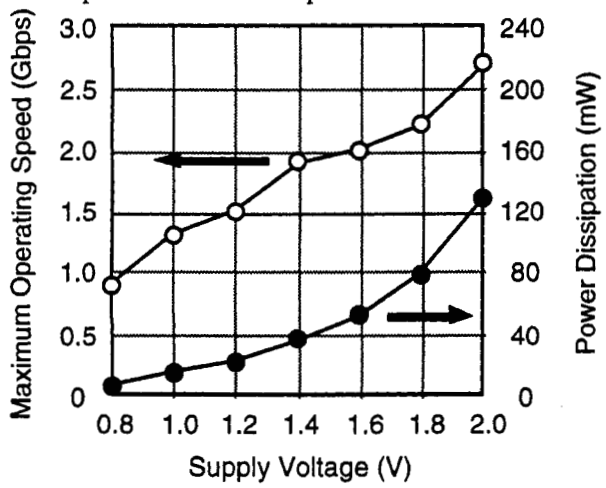


Fig. 10 Speed and Power of 1:4 demultiplexer.

IV. Conclusion

We have developed a 4:1 multiplexer and a 1:4 demultiplexer for ultra high-speed telecommunication system LSIs. The multiplexer adopted a shift register architecture with a modified counter operating stably at high-speeds, while the demultiplexer adopted a 2-bit tree architecture. We adopted a double-rail flip-flop circuit operating at high-speed to both the multiplexer and the demultiplexer. With 0.35μm SOI-CMOS circuit technology, the multiplexer operated at 2.0Gbps dissipating 122mW and the demultiplexer ran at 2.7Gbps with 128mW at a 2.0V supply voltage.

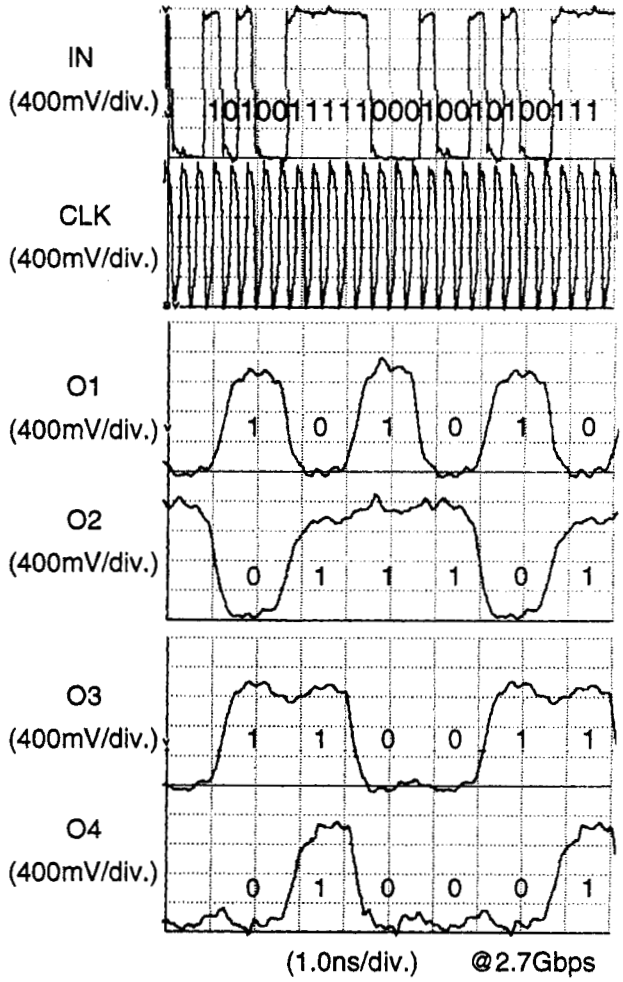


Fig. 11 Operating waveforms of 1:4 demultiplexer.

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