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On-chip di/dt Detector IP for Power Supply

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Abstract — This paper demonstrates an on-chip di/dt detector IP. The di/dt detector core consists of a power supply line, an underlying spiral inductor and an amplifier. The mutual inductor induces a di/dt proportional voltage, and the amplifier amplifies and outputs the value. The measurement results show that the di/dt detector output and the voltage difference between a resistor have good agreement.

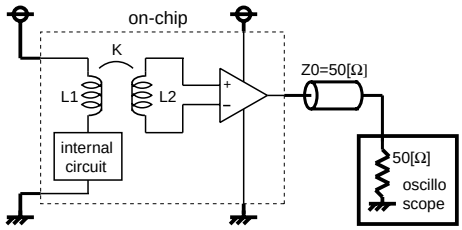

Figure 1: Block diagram of the di/dt detector circuit. The bold lines represent outside devices.

1 Introduction

As the process technology advances, the number of the transistors on an LSI chip has been increasing and their high speed operations generate more power supply noise while the low supply voltage reduces the noise margin. Thus, the power supply noise becomes a serious issue for the reliability of the LSI operations.

Recently, a di/dt noise is becoming one of the dominant source of the power supply noise along with an IR drop. An EMI noise also becomes a serious problem for high speed operating LSIs. Therefore, a current measurement technique, especially a high frequency di/dt measurement technique, is necessary in order to estimate the di/dt noise.

Many techniques have been proposed to measure the power supply voltage bounce[1]. On the other hand, only few techniques have been developed for the power supply current measurement. One technique uses a resistor connected in series to a power supply line on a PCB board and measures the voltage difference of the both terminals using electron-beam probing[2]. This technique needs numerical calculation to obtain the current and di/dt waveforms. Another technique picks up the magnetic field and measure the spectrum[3]. It is unable to reproduce the original current nor di/dt waveforms from the spectrum because the phase information is lost.

This paper demonstrates an on-chip di/dt detector IP[4]. This IP can be applicable for feedback substrate noise cancelling[5], feedback di/dt noise control[6] and so on because the detector is realized on-chip and outputs the di/dt value in real time.

2 Circuit Design

2.1 Basic Concept

Figure 1 shows the block diagram of the di/dt detector circuit. A power supply current for the internal circuit goes through the power supply line inductance L_1. A pickup inductance L_2 coupled to L_1 with a coupling coefficient K induces a di/dt proportional voltage. A noise-tolerant amplifier amplifies the induced voltage and outputs to a 50Ω transmission line that enables a high frequency measurement. The detailed circuit with the measurement setup is shown in Fig.2.

2.2 Mutual Inductor

The inductance L_1 should be small since it is in series connection to the power supply line. The small inductance requires a high coupling coefficient K and a bigger L_2 in order to generate the enough induced voltage on the terminal of L_2. The mutual inductor consists of the power supply line and an underlying spiral inductor. The power supply line has straight layout with

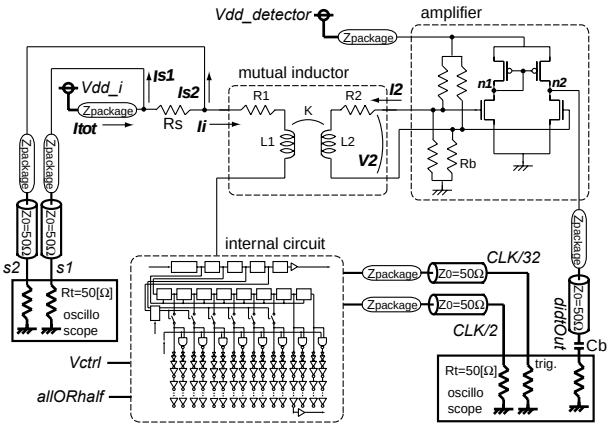

Figure 2: Over-all circuit with the measurement setup.

80μm width using ML2 and ML3 together to reduce the parasitic impedance. The spiral inductor has 20 turns with 200μm diameter, 2μm width and 2μm spacing using ML1, as shown in Fig.3. The equivalent circuit is included in Fig.2.

2.3 Amplifier and Output buffer

Since the output di/dt value is a high speed analog signal, a high frequency and high linearity amplification is the key issue for the amplifier design. The amplifier schematic is also shown in Fig.2. We employ a current mirror type amplifier without current source. The resistors R_b are used to keep the DC bias voltage as half-vdd. The resistance is big enough to be considered open for AC signal.

The output is connected to a transmission line whose characteristic impedance is 50Ω. The blocking capacitor C_b is inserted at the input port of the oscilloscope to prevent the bias point change of the node $n2$ due to the 50Ω termination resistor connected to GND. Note that the average of di/dt value is zero because the current value is finite, so that the blocking capacitor does not affect the measurement.

2.4 Overview and Measurement Setup

As shown in Fig.2, the power supply line has an on-chip resistor R_s in series, the both terminals of which are connected to output pins as $s1$ and $s2$ in order to enable the current measurement by calculating the voltage difference, and compare the result with the di/dt detector output as a reference.

3 Analytical Model

3.1 Equations

The mutual inductance $M = K\sqrt{L_1 L_2}$. Assuming that the internal current is I_i and the input current of the amplifier is I_2, the output voltage of the mutual inductor V_2 is

$$V_2 = M\frac{dI_i}{dt} + R_2 I_2 + L_2\frac{dI_2}{dt} \approx M\frac{dI_i}{dt}. \quad (1)$$

Here I_2 is small enough because the input impedance is large enough compared with R_2 and ωL_2 ($\omega \ll 10$GHz).

Assuming that the gain of the amplifier is G, the output voltage $V_{didtOut}$ of the di/dt detector circuit is

$$V_{didtOut} = GV_2 = GK\sqrt{L_1 L_2}\frac{dI_i}{dt} \quad (2)$$

which means

$$\frac{dI_i}{dt} = \frac{1}{GK\sqrt{L_1 L_2}}V_{didtOut} \equiv A_{v2didt}V_{didtOut} \quad (3)$$

where

$$A_{v2didt} \equiv \frac{1}{GK\sqrt{L_1 L_2}}. \quad (4)$$

Integrating eqn(3) with respect to time,

$$I_i = A_{v2didt}\int V_{didtOut}dt + C. \quad (5)$$

The relation between the internal current I_i and the voltage of $s1$, $s2$ is

$$V_{s1} - V_{s2} = R_s(I_i + I_{s2}) \quad (6)$$

and this equation can be converted to

$$V_{s1} - \left(1 + \frac{R_s}{R_t}\right)V_{s2} = R_s I_i \quad (7)$$

using $I_s = V_s/R_t$, where R_t is the termination resistance 50Ω. From eqn(5) and (7),

$$V_{s1} - \left(1 + \frac{R_s}{R_t}\right)V_{s2} = R_s A_{v2didt}\int V_{didtOut}dt + C. \quad (8)$$

Differentiate eqn(8) by time,

$$V_{didtOut} = \frac{1}{R_s A_{v2didt}}\frac{d\{V_{s1} - (1 + R_s/R_t)V_{s2}\}}{dt}. \quad (9)$$

3.2 Designed Parameters

The equivalent circuit of the mutual inductor is extracted using FastHenry 3D field solver as L_1=0.26nH, R_1=0.14Ω, L_2=52.3nH, R_2=212Ω and K=0.25.

According to HSPICE simulations, the gain of the amplifier G is 0.76, the cut-off frequency is 3.3GHz when no load capacitance, and the output linearity range is about ±0.35V.

The series resistor R_s on the power supply line is formed using gate-poly with silicide, and the designed resistance value is about 2.3Ω. The bias resistor R_b is formed using gate-poly without silicide and the designed value is about 10kΩ.

4 Measurement Results

4.1 Setup

The chip was designed and fabricated using 0.35μm 2-Poly 3-ML standard CMOS technology. The chip area is 3.0mm×1.8mm and the chip photograph is shown in Fig.3. The area of the di/dt detector core is 340μm×280μm.

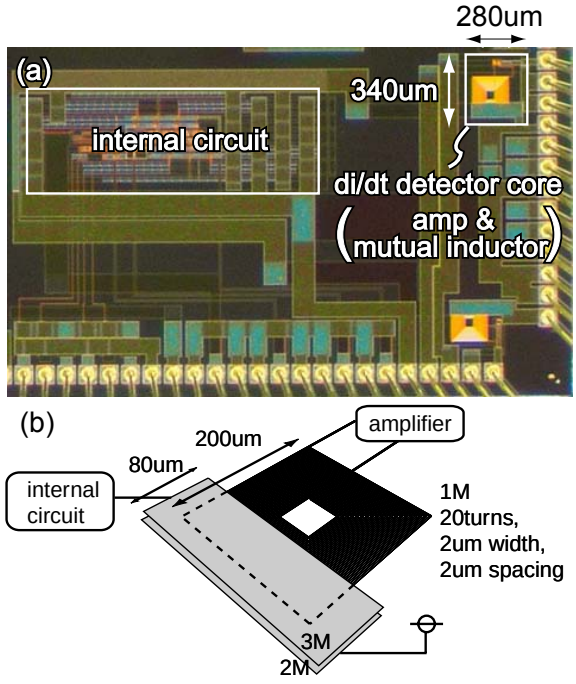

Figure 3: (a) Chip photograph. The chip area is 3.0mm×1.8mm. The area of the di/dt detector core is 340μm×280μm. (b) Mutual inductor structure.

4.2 Sensitivity of the di/dt detector

Figure 4 shows the waveforms of (a) $CLK/2$, $s1$ and $s2$, (b) $V_{s1} - (1 + R_s/R_t)V_{s2}$ signal and the numerical-time-integral of the di/dt detector output multiplied by $R_s A_{v2didt}$, based on eqn(8), (c) the di/dt detector output and the numerical-time-differential of $V_{s1} - (1 + R_s/R_t)V_{s2}$ signal divided by $R_s A_{v2didt}$, based on eqn(9). Since the $V_{s1} - (1 + R_s/R_t)V_{s2}$ waveform is noisy, we applied a smoothing before the numerical differentiation. The (M) and (C) in the signal caption represent the measured and calculated waveforms, respectively. The current and di/dt values on the right vertical axis in the graph (b) and (c) are calculated using R_s=2.04Ω and A_{v2didt}=1.43×10^9, respectively.

These graphs show that the currents measured by the series resistor voltage difference and the di/dt detector output have good agreement, and our di/dt detector circuit works well.

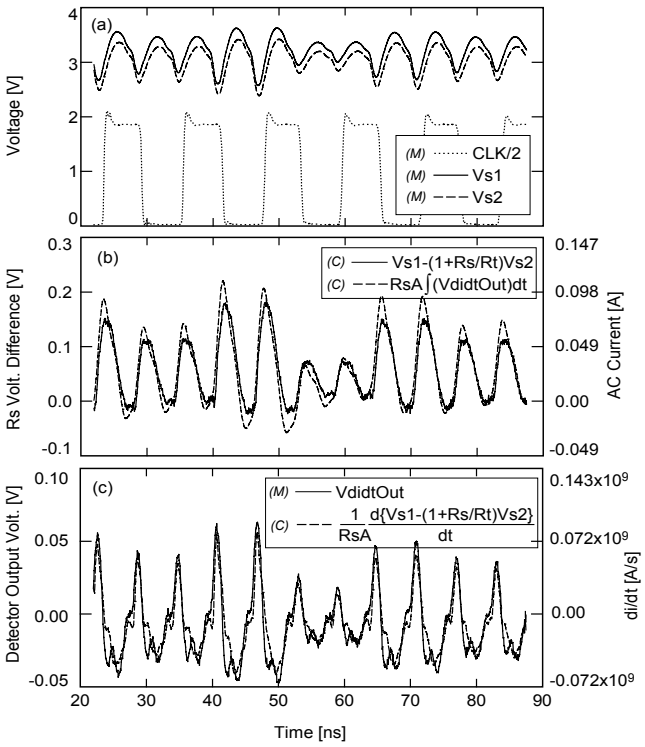

Figure 4: Waveforms of (a) $CLK/2$, $s1$ and $s2$, (b) Current waveforms, (c) di/dt waveforms.

4.3 Accuracy of the di/dt detector

The series resistance value R_s can be estimated from $s1$ and $s2$ voltage difference. Since the internal circuit does not consume current at the time just before the CLK edge under a low speed operation because of no

switching, the DC current going through the series resistor is the same as the current going into the termination resistor R_t of $s2$, and $I_{s2} = V_{s2}/R_t$. The series resistance value is evaluated by $R_s = \Delta V/I_{s2} = R_t \Delta V/V_{s2} =$ 2.04Ω. The designed value R_s=2.3Ω is a rough estimation, and the measured value 2.04Ω is reasonable.

The error between the solid lines and the dashed lines in Fig.4(b) and (c) are evaluated by the standard deviation,

$$\sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(V_{solid} - V_{dashed})^2} \qquad (10)$$

from 22ns to 72ns region, and the number of the sampling points N is about 750. The error in the graph (b) is σ=9.10mV which corresponds to 4.46mA, and the error in the graph (c) is σ=6.30mV which corresponds to 9.01mA/ns.

4.4 Input Impedance of the di/dt detector

The primary part L_1 and R_1 of the mutual inductor is inserted in series to the power supply line, and the impedance disturbs the power supply voltage for the internal circuit. According to an HSPICE simulation using the parasitic impedance extracted by FastHenry and the current waveform shown in Fig.4(c) dashed line, the voltage drop between the terminal is about 15mV which is acceptable for real applications.

4.5 Constraint

The followings are the constraint of our di/dt detector IP. 1) Frequency response of the amplifier ($\omega_{cut} > \omega_{didt}$). 2) Impedance of the secondary spiral and the load capacitance ($|R_2 + j\omega_{didt}L_2| < 1/\omega_{didt}C_{load}$). 3) Resonance frequency of the secondary spiral inductance and the load · parasitic capacitance ($\omega_{didt} < 1/\sqrt{L_2 C}$). Here, the load capacitance means the input capacitance of the amplifier. The parasitic capacitance includes the capacitance of the secondary spiral — the substrate, and the capacitance between the adjacent spiral wires.

5 Conclusion

The on-chip di/dt detector IP has been demonstrated. The measurement results show that the di/dt detector output and the voltage difference between a resistor have good agreement with the accuracy of 9.01mA/ns. The characteristics of this IP is summarized in Table1.

Table 1: Characteristics of the di/dt detector IP

area	280μm×340μm
pin count	3 (di/dt output, Vdd·Gnd for amp.)
input impedance	R=0.14Ω, L=0.26nH
accuracy	10mA/ns
measurable range	±500mA/ns
measurable freq.	f_{cut}=3.3GHz

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