PAPER

Autonomous di/dt Control of Power Supply for Margin Aware Operation

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SUMMARY This paper demonstrates an autonomous di/dt control of power supply for margin aware operation. A di/dt on the power line is detected by a mutual inductor, the induced voltage is multiplied by Gilbert multiplier and the following low pass filter outputs a DC voltage in proportion to the di/dt. The DC voltage is compared with reference voltages, and the modes of the internal circuit is controlled depending on the comparators output. By using this scheme, the di/dt noise power can be autonomously controlled to fall within a defined range set by the reference voltages. Our experimental results show that the internal circuit oscillates between the all-active and the half-active modes, also show that the all/half ratio and the oscillation frequency changes depending on the reference voltages. It proves that our autonomous di/dt noise control scheme works as being designed.

key words: *autonomous di/dt control, margin aware, di/dt detector, power supply current*

1. Introduction

As the process technology advances, the number of transistors on an LSI chip has been increasing and their high speed operations generate more power line noise while the low supply voltage reduces the noise margin. The power line noise becomes a serious issue for the reliability of the LSI operations. The noise on a power line is caused by di/dt noise and resistive voltage drops due to the parasitic impedance of the power line. As a chip operating frequency becomes higher, the $L(di/dt)$ noise becomes dominant over the IR drop. Since the ground line and the substrate are tied with very low impedance, the ground line noise presents on the substrate [1] as well and becomes a serious concern on analog-digital mixed signal LSIs. An EMI noise is also caused by the di/dt. Therefore the di/dt control is a key technique for improving the signal integrity issue on high-frequency operating LSIs.

It is difficult to predict the amount of the di/dt noise by a circuit simulation because it requires a huge database of the parasitic impedance, the switching activity and the switching timing, along with very long simulation time. In addition, many recent LSIs have several operating modes. Moreover, a process variation often makes the prediction different from the actual di/dt noise [2].

This paper proposes an autonomous and margin aware di/dt noise control scheme. We have proposed an on-chip di/dt detector [3], and an active substrate noise cancelling technique using the di/dt detector [4]. The di/dt detector can also be used for the di/dt noise control scheme since the detector is realized on-chip and outputs the di/dt value in real time. The autonomous and margin aware di/dt noise control scheme is demonstrated here using 0.15 μm 5-ML SOI-CMOS technology [5].

Section 2 presents the basic concept and the circuit design. Measurement results are shown in Sect. 3, and Sect. 4 discusses the results. Then Sect. 5 concludes this paper.

2. Circuit Design

2.1 Basic Concept

The block diagram of the autonomous di/dt noise control scheme is shown in Fig. 1. The operation of the internal circuit causes the di/dt of the power line. The mutual inductor induces the di/dt proportional voltage between the terminals of the secondary inductor, the induced voltage is squared and the di/dt noise power waveform is obtained. And the following low pass filter outputs the DC voltage in proportion to the di/dt noise power. Then the DC voltage is compared with reference voltages. The di/dt generation of the internal circuit is controlled by changing the operation mode in accordance with the comparator outputs. For example, the modes of the internal circuit include the variations of the clock frequency, effective power supply voltage, threshold voltage, number of the pipeline stage, number of parallel threading and so on. By using this feedback, we can control the amount of di/dt generation by setting the reference voltages.

The advantage of this technique are that this is a measurement based so that the process, voltage and temperature variation are automatically taken into account, the prediction of di/dt generation by time-consuming circuit simula-

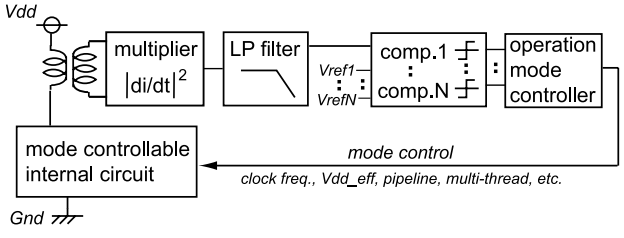

Fig. 1 Block diagram of the autonomous di/dt noise control scheme.

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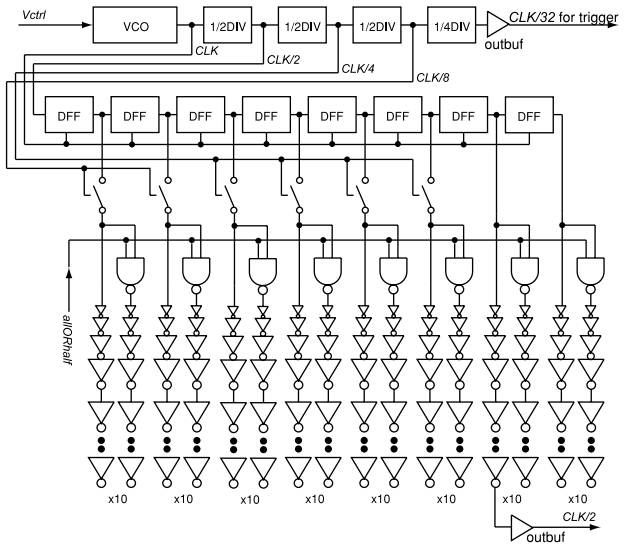

Fig. 2 Internal circuit.

tion is not necessary, we can get a best effort performance under the restricted di/dt range, the allowed di/dt range is easily controllable by the reference voltages, and it is expected that a decided noise margin is autonomously realized by setting the proper reference voltages.

2.2 Internal Circuit as Noise Source

Figure 2 shows our internal circuit as a noise generator. The circuit contains VCO so that we can easily sweep the clock frequency by changing the DC control voltage ($Vctrl$). The frequency divider generates 101010... signal for the input to the shift resister. The following dividers generates $CLK/4$, $CLK/8$ signals by which the DFF outputs and some inverter chains are disconnected when the divided clock outputs are "Low," and hence the current waveform becomes different in accordance with the divided clock signals. The $CLK/32$ output is used as a trigger for a oscilloscope, and the $CLK/2$ output is used to check if the circuit works fine. $allORhalf$ signal changes the activation ratio of the circuit. Thus the internal circuit has two modes, the all-active and half-active modes. The half-active mode generates less di/dt since half of the circuit is turned off. The all-active mode represents high-performance mode, and the half-active represents low-noise mode.

2.3 di/dt Detector

The di/dt detector here is a mutual inductor which induces the di/dt proportional voltage between the terminals. The mutual inductors here consists of a power supply line and an underlying spiral inductor. The power supply line L_1 is composed of the top metal layer ML5 with 1 turn, 20 μm width. The spiral inductor L_2 has 20 turns with 2 μm width and 2 μm spacing using ML3. The outside diameter of the both inductors are 150 μm $\times$ 150 μm. The equivalent circuit of the spiral is extracted using FastHenry 3D field solver

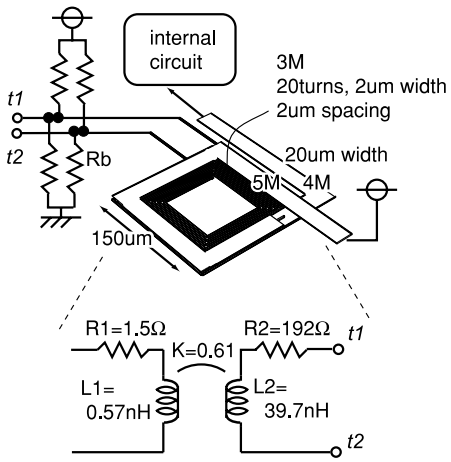

Fig. 3 Mutual inductor structure.

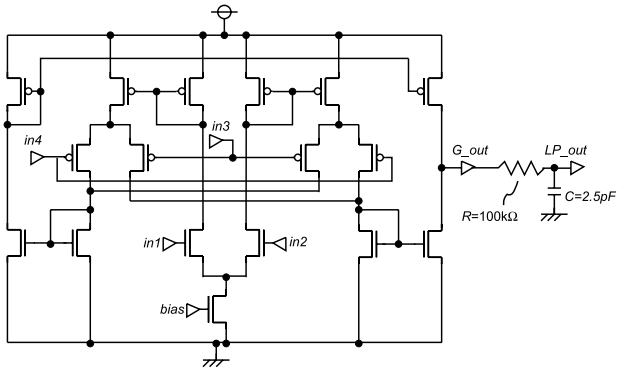

Fig. 4 Gilbert multiplier and low pass filter.

[7], as shown in Fig. 3, and the impedance are L_1=0.570 nH, L_2=39.7 nH, K=0.611, R_1=1.5 Ω, R_2=192 Ω.

The resistors R_b are used to keep the DC bias voltage as half-Vdd for the following input. The resistor is formed using gate-poly without silicide and the resistance is 10 kΩ which is big enough to be considered open for AC signal.

2.4 di/dt Multiplier and Low Pass Filter

A Gilbert multiplier [6] is used for obtaining the square of the di/dt signal, which converts the di/dt proportional voltage into the di/dt noise power waveform. The following low pass filter is composed of a resistor and a capacitor. The schematic is shown in Fig. 4.

The analog output current of the multiplier is proportional to $(V_{in1} - V_{in2}) \times (V_{in3} - V_{in4})$. Here, $in1$ and $in3$ in Fig. 4 are connected to $t1$ in Fig. 3, and $in2$, $in4$, $t2$ are connected so that the output signal is proportional to the di/dt noise power. The gain of the Gilbert multiplier is G=3.87 according to an HSPICE simulation.

The resistor of the low pass filter is formed using gate-poly without silicide and the resistance is about 100 kΩ, the capacitor is formed using MIM capacitor and the capacitance is about 2.5 pF.

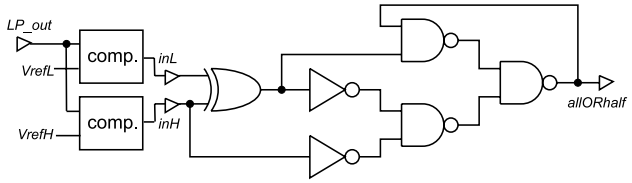

Fig. 5 Schematic of the operation mode controller.

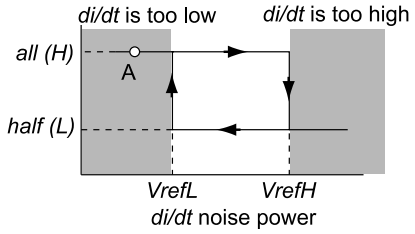

Fig. 6 Operation of the hysteresis comparator.

2.5 Comparators and Operation Mode Controller

The comparator compares the di/dt noise power voltage with the reference voltage, and outputs "H" if the di/dt noise power voltage is higher than the reference voltage. We use two comparators with two reference voltages as V_{refL} and V_{refH}. The schematic of the operation mode controller is shown in Fig. 5.

The internal circuit has two modes, the all-active high-performance mode and the half-active low-performance mode. When the di/dt noise power is too high ($V_{LPout} > V_{refH}$ and inL=inH="H"), the mode controller outputs "L" to change the mode into the half-active mode where the half of the internal circuit is turned off and the di/dt is reduced. When the di/dt is low enough ($V_{LPout} < V_{refL}$ and inL=inH="L"), the mode controller outputs "H" to change the mode into the all-active mode where all the internal circuit is turned on. When the di/dt noise power is between V_{refH} and V_{refL}, the operation mode controller outputs the signal so as to keep the previous operation mode. Thus, the comparators and the operation mode controller consist of a hysteresis comparator, as shown in Fig. 6.

3. Measurement

3.1 Setups

The chip is designed and fabricated using 0.15 μm 5-ML SOI-CMOS technology, and the chip area is about 3.2 mm × 1.8 mm, as shown in Fig. 7.

The chip is mounted on a Cu board as shown in Fig. 8. All the inputs are DC and supplied through lead lines to the "islands" on the board. The voltage of the islands are stabilized by several chip capacitors. 50 Ω transmission lines are directly connected to the high-speed output pins including $CLK/2$, $CLK/32$. The $allORhalf$ signal is probed by a high impedance (1 MΩ) probe.

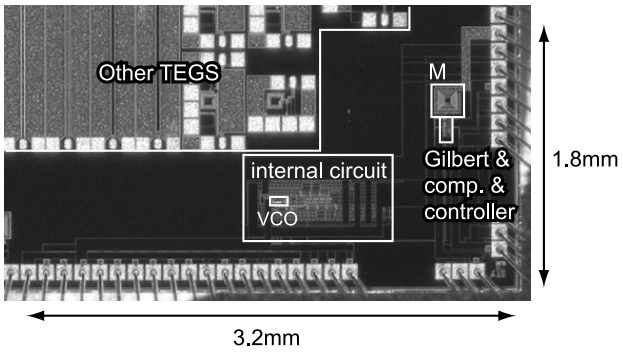

Fig. 7 Chip photograph.

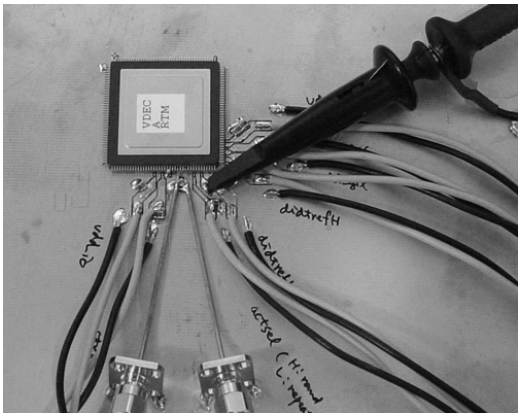

Fig. 8 Measurement setup.

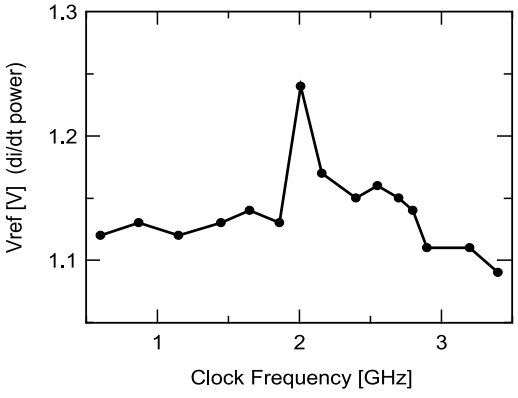

Fig. 9 Clock frequency dependence of the di/dt noise power.

3.2 Frequency Dependence of di/dt Noise Power

When the same reference voltage is applied to V_{refH} and V_{refL}, and sweeping the reference voltage, the $allORhalf$ signal changes when the reference voltage crosses the low pass filter output voltage which reflects the di/dt noise power. (Actually $allORhalf$ oscillates at a range of the reference voltage, which will be described in the next section, the center voltage is used here as the low pass filter output voltage, and hence the di/dt noise power.)

The clock frequency dependence of the di/dt noise power under 1.5 V power supply is shown in Fig. 9. It shows that the di/dt noise power has a peak at around 2.0 GHz, which reflects the package and the bonding wire characteristics.

4. Discussions

4.1 Waveforms of Oscillation

As being described, the internal circuit has two modes: the all-active and half-active modes. If V_{refH} is set lower than the di/dt noise power of the all-active and V_{refL} is set higher than the di/dt noise power of the half-active mode, the internal circuit oscillates between the two modes.

Let's start from the point A in Fig. 6. Since the circuit is operating in all-active mode, the low pass filter output voltage V_{LPout} is getting higher toward the di/dt power operating in the all-active mode V_{all} with the low pass filter time constant, until hitting to V_{refH}. Then the mode turns to half-active mode, the voltage is getting lower toward the di/dt power operating in the half-active mode V_{half}, until hitting to V_{refL}, then turns to the all-active mode, and going around the hysteresis curve. Here, the di/dt power of the all-active mode and of the half-active mode (V_{all} and V_{half}) is decided, while the setting of V_{refH} and V_{refL} changes the oscillation conditions, as shown in Fig. 10 which describes the transient response of the low pass filter output voltage. The oscillation frequency depends on the reference voltage difference $\Delta V_{ref}(= V_{refH} - V_{refL})$ and the low pass filter time constant. A bigger reference voltage difference leads longer oscillation period. The H/L ratio depends on the average of the reference voltages $(V_{refL} + V_{refH})/2$, and higher reference voltages lead higher H ratio, and the higher H ratio leads higher average output voltage of V_{out}, as shown in Fig. 10. The voltage of the $allORhalf$ was probed as V_{out}, and the measured oscillation waveforms between the all-active(H) and the half-active(L) modes at some reference voltage conditions are shown in Fig. 11. The internal clock frequency is set to 2.0 GHz in this measurement where the maximum di/dt is obtained as shown in Fig. 9.

The applied reference voltages, the measured H/L ratio and the oscillation period of (a), (b), (c) and (d) cases of Fig. 11 are summarized in Table 1. Since the output driver of the $allORhalf$ signal is so small that the average output voltage V_{out} is used here as the indication of the H/L ratio. For the H/L ratio, though the difference of case (b) and (c)

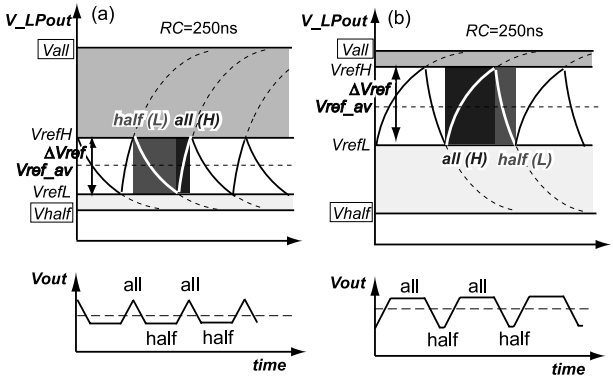

Fig. 10 Transient response of the low pass filter output. A bigger reference voltage difference (ΔV_{ref}) leads longer oscillation period, and higher reference voltages (V_{ref_av}) lead higher H ratio, resulting higher output voltage of V_{out}.

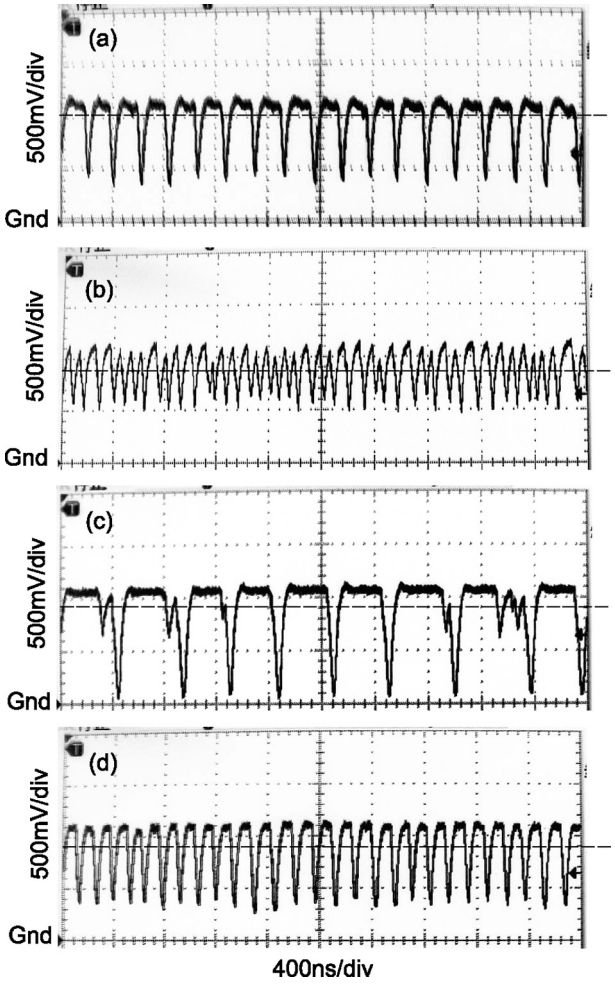

Fig. 11 Measured oscillation waveforms of $allORhalf$ signal at 2.0 GHz internal clock frequency. The applied reference voltages, the measured results are summarized in Table 1.

Table 1 The reference voltage dependence of the H/L ratio (upper). and the oscillation period (lower). Higher V_{out} means higher H ratio.

	V_{ref_av}[V]	ΔV_{ref}[V]	V_{out}[V]	period [ns]
(a)	1.275	0.01	1.0	222
(b)	1.270	0.00	0.9	91
(c)	1.270	0.02	0.9	444
(d)	1.265	0.01	0.9	148

	V_{ref_av}[V]	ΔV_{ref}[V]	V_{out}[V]	period [ns]
(b)	1.270	0.00	0.9	91
(d)	1.265	0.01	0.9	148
(a)	1.275	0.01	1.0	222
(c)	1.270	0.02	0.9	444

is not clear because the ΔV_{ref} is not the same, the difference between (a) and (d) is clear and reasonable as shown in Table 1 upper. For the oscillation period, it is clear that the oscillation period becomes longer as ΔV_{ref} becomes larger as shown in Table 1 lower.

No oscillation occurs and stays "L" when $V_{refL} \leq 1.25$V and stays "H" when $V_{refH} \geq 1.29$V because the all-active mode has the di/dt noise power of 1.29-δ[V] and half-active mode has the di/dt noise power of 1.25+δ[V] where $0 < \delta < 0.01$V.

Here, note that the oscillation is undesired operation in a real application. We intended to generate and measure the oscillation in order to demonstrate that our autonomous di/dt control works as being designed.

4.2 Practicality

The impedance of the di/dt detector itself may cause additional power supply noise for the internal circuit since the primary part is in series to the power supply line. We have to pay much attention especially when chips are mounted using SIP or flip-chip techniques in which the original parasitic impedance is very small. Since this is a feasibility experiment, we employed a conservative design on the mutual inductor structure. However, the power supply noise can be reduced with smaller resistance R_1 and inductance L_1 by using a thicker metal or multi-layer, wider and straight power supply line with an adjacent spiral inductor [3]. As for the EMI noise, the di/dt generation control is effective regardless of the power supply voltage fluctuation.

Most of real chips including ASICs, microprocessors and so on, have many power supply pins. In this case, di/dt controller can be inserted to each pin, or be inserted to dominant pins on which large currents flow.

It is natual for recent LSIs to have multi operation mode, such as high-performance mode and low-power mode. As the signal integrity is becoming serious issue, this paper proposes to add the low-noise mode. That is, it is important to think of a trade-off between performance, power dissipation and noise generation as well.

5. Conclusions

An autonomous and margin aware di/dt noise control scheme has been demonstrated. A di/dt on the power line is detected by a mutual inductor, the induced voltage is squared by the Gilbert multiplier and the following low pass filter outputs the DC voltage in proportion to the di/dt noise power. The DC voltage is compared with reference voltages, and the mode of the internal circuit is controlled depending on the comparators output. By using this scheme, the di/dt noise power can be autonomously controlled to fall within a defined range set by the reference voltages. The advantage of this technique are that this is a measurement based so that the process, voltage and temperature variation are automatically taken into account, the prediction of di/dt generation by time-consuming circuit simulation is not necessary, we can get a best effort performance under the restricted di/dt range, the allowed di/dt range is easily controllable by the reference voltages, and it is expected that a decided noise margin is autonomously realized by setting the proper reference voltages. Though we used only two operation modes in this study, it can be easily extended to multiple operation modes.

Our experimental results show that the internal circuit oscillates between the all-active and the half-active modes, also show that the all/half ratio and the oscillation frequency changes depending on the reference voltages. It proves that our autonomous di/dt noise control scheme works as being designed.

This is the first demonstration, as the authors knowledge, of an autonomous and margin aware di/dt noise control scheme.

Acknowledgments

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