PAPER Special Section on Papers Selected from AP-ASIC 2004

# **Preliminary Experiments for Power Supply Noise Reduction Using On-Board Stubs**

Toru NAKURA<sup>†a)</sup>, Student Member, Makoto IKEDA<sup>††</sup>, and Kunihiro ASADA<sup>††</sup>, Members

**SUMMARY** This paper demonstrates a power supply noise reduction using on-board stubs. A quarter-length stub attached to the power supply line of an LSI chip works as a band-eliminate filter, and suppresses the power supply noise of the designed frequency. Preliminary experiments show that 87% of the designed frequency noise component is suppressed when stub patterns are written on a power supply area on a PCB board for a 1.25 GHz operating LSI. The results show the possibility of the stub on-chip integration when the operating frequency of LSIs becomes higher and the stub length becomes shorter.

key words: stub, on-board, power supply noise, di/dt noise, PRBS pattern

#### 1. Introduction

As the process technology advances, the number of transistors on an LSI chip has been increasing and their high speed operation generates more power supply noise while the low supply voltage reduces the noise margin. Thus, the power supply noise becomes a serious issue for the reliability of the LSI operations.

Recently, a di/dt noise is becoming one of the dominant source of the power supply noise along with an IR drop. An EMI noise caused by the di/dt also becomes a serious problem for high speed operating LSIs. In order to suppress the di/dt, some methods, such as a semi-asynchronous architecture [1] and an inserting decoupling capacitor method [2] have been proposed. However, these methods make the circuit design complex and difficult, and an on-chip decoupling capacitor requires more die area, an off-chip decoupling capacitor does not work well due to the parasitic inductance on the terminal.

Stubs are widely used for impedance matching technique of wireline communications, and we proposed to use the stubs for power supply noise reduction. We have theoretically shown that stubs attached to a power supply line of an LSI can reduce the power supply noise, and stubs will work more efficiently as the operating frequency of the LSI becomes higher [3], [4]. This paper describes the first experimental results, as the authors knowledge, of power supply noise reduction [5] using on-board stubs for a real LSI chip.

In Sect. 2, the basic stub theorem and the analytical models are presented. Section 3 describes the setup for the

<sup>†</sup>The author is with the Dept. of Electronic Engineering, The University of Tokyo, Tokyo, 113-8656 Japan.

a) E-mail: nakura@silicon.t.u-tokyo.ac.jp

DOI: 10.1093/ietele/e88-c.8.1734

measurement. Experimental results will be shown in Sect. 4. Discussions are given in Sect. 5, and Sect. 6 concludes this paper.

## 2. Theorem

As the operation frequency becomes higher and the wavelength of voltage and current gets comparatively smaller with the interconnect wire length, the wires should be considered as transmission lines instead of lumped RC elements. The characteristic impedance  $Z_0$  and the phase constant  $\beta_c$  of the transmission lines are

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{1}$$

$$\beta_c = -j\sqrt{(R+j\omega L)(G+j\omega C)}$$
(2)

where R, L, G, C are the resistance, inductance, admittance representing the dielectric loss, capacitance of the wire, per unit length respectively.

The input impedance of the transmission line with its length l and the termination impedance  $Z_l$  is

$$Z_{stub} = Z_0 \frac{Z_l \cos \beta_c l + j Z_0 \sin \beta_c l}{Z_0 \cos \beta_c l + j Z_l \sin \beta_c l}.$$
(3)

When open termination ( $Z_l = \infty$ ), and if the transmission line has no loss (R = G = 0) and its length is quarter of the signal wavelength ( $\beta_c l = \pi/2$ ), the input impedance of the stub becomes zero ( $Z_{stub} = 0$ ), which is equivalent with infinite capacitance. When this stub is attached to the power supply line, the voltage fluctuation is suppressed.

The dominant frequency of the switching currents is the operating frequency  $f_0$ . Thus, the stub length adjusted for the operating frequency becomes

$$l = \frac{\pi/2}{\beta_{r0}} = \frac{\lambda_0}{4} = \frac{c/\sqrt{\epsilon_{reff}}}{4f_0} \tag{4}$$

where  $\lambda_0$ , *c* and  $\epsilon_{reff}$  are the signal wavelength in the transmission line, the speed of light in vacuum and the effective dielectric constant. Since the stub input impedance is kept to be small around  $f_0$ , the stub suppresses the noise of around the  $f_0$  components as well. The bandwidth is decided by the stub parameters *R*, *L*, *G*, *C* and the frequency  $f_0$ .

Since the maximum operating frequency of our test chip is about 2 GHz and the stub length becomes over 15 mm in SiO<sub>2</sub>, it is too long to realize the stub on-chip and we use on-board stubs here as a preliminary experiment.

Manuscript received November 17, 2004.

Manuscript revised February 7, 2005.

<sup>&</sup>lt;sup>††</sup>The authors are with the VLSI Design and Education Center (VDEC), The University of Tokyo, Tokyo, 113-8656 Japan.

## 3. Setups

#### 3.1 Test Circuit

A PRBS (Pseudo Random Bit Stream)  $2^7 - 1$  generation circuit with an inverter chain at each output of the DFF is used as our test circuit, as shown in Fig. 1. This circuit represents common synchronous circuits. The PRBS pattern and the inverter chains represent the random switching of an LSI and the combination logics, respectively. The length of the inverter chains distributes from 2 to 12, which represents a path length distribution between DFFs.

The test circuit contains VCO so that we can easily sweep the operating frequency by changing the DC control voltage (*Vctrl*). The selector circuit selects the random mode which uses the feedback from the XOR gate, and the repeat mode which uses the *CLK*/2 signal, to the input of the shift register. The repeat mode is the optimistic case and the random mode is the pessimistic case from the stub noise reduction point of view. Note that the power supplies for the internal circuit and for the IO buffers are isolated.

The circuit is designed and fabricated using  $0.18 \,\mu\text{m}$  5ML standard CMOS technology, as shown in Fig. 2. The size of the test circuit is about  $2 \,\text{mm} \times 0.5 \,\text{mm}$ .

## 3.2 Measurement Setup

The chip is assembled in 160 pin QFP package and it is



**Fig.1** Internal circuit. A PRBS generator and inverter chains. *SEL* signal selects the repeat mode or the random mode.



Fig. 2 Chip photograph.  $0.18 \,\mu\text{m}$  5ML CMOS,  $2 \,\text{mm} \times 0.5 \,\text{mm}$ .

mounted on a Cu board as shown in Fig. 3, and the corresponding schematic is shown in Fig. 4. The DC bias of *Vdd*, *Vddio*, *Vctrl* and *SEL* are supplied through lead lines to the islands on the board. The voltage of the islands are stabilized by several chip capacitors. The *Vddn* island which is the power supply for the internal circuit through *Vdd\_internal* pin is connected to the *Vdd* island by a wire and has no chip capacitor. The parasitic inductance of the wire causes noise voltage to the *Vddn* island. The power supply voltage here is 3.0 V for high speed operation of the circuit.

Two types of the Vddn island has been tested. One is "w/o stubs" which is 4.7 mm × 10.0 mm rectangle, the other is "with stubs" which has 1.25 GHz and 1.95 GHz stubs attached to the "w/o stubs" rectangle. The voltage of the Vddn island is directly probed by 50  $\Omega$  transmission line so that the power supply noise can be measured by the spectrum analyzer and the oscilloscope. Other 50  $\Omega$  transmission lines are also connected to the *CLK/32* and *PRBS* output pins of the test chip, and connected to the oscilloscope.

3.3 Stub Design

The stub frequencies are around 1.25 GHz and 1.95 GHz in our experiment. The stub patterns are written on the surface of the PCB board whose dielectric material is 1 mm



Fig. 3 Photograph of the chip mount, (a) w/o stubs, and (b) with stubs.



Fig. 4 Schematic of the measurement setup.

thickness FR4 ( $\epsilon_r$ =4.8) sandwiched by 18  $\mu$ m cupper films. The stubs are composed of microstrip line with the width of 1 mm, and the effective dielectric constant becomes [6]

$$\epsilon_{reff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left( 1 + \frac{12h}{w} \right) = 3.427 \tag{5}$$

if only the cupper film is removed. However, the stub patterns are written by scratching the FR4 with dozens of micron meter depth as well as the cupper film and hence the effective dielectric constant becomes smaller. Also, the dielectric constant of FR4 has frequency dependence and it becomes lower as the frequency becomes higher [6]. The edge effects affect the stub frequencies as well. Section 2 assumes that L, C are constant along the stub with an open termination, however, the actual L, C values become different around the stub edges, also the termination is not completely open. By accounting these issues, the effective dielectric constant in this experiment is calculated as 2.67 for Eq. (4) from the measurement results that the measured stub frequencies are 1.25 GHz and 1.95 GHz, and the stub length are 36.7 mm and 23.5 mm.

## 4. Measurement Results

# 4.1 S-Parameter

The stub frequency characteristics are measured by a network analyzer. The "w/o stubs" and "with stubs" patterns are fabricated on a Cu board, and SMA connectors are soldered on the patterns, as shown in Fig. 5. The calibration is conducted from the port 1 and port 2 of the network analyzer to the end of the 50  $\Omega$  cables using 3.5 mm (SMA compatible) standard 50  $\Omega$ , open and short terminators. Then the cables are connected to the SMA connectors on the patterns and the S-parameters are measured.

Figure 6 shows the transmission characteristics ( $S_{21}$ ) of the *Vddn* island of the with/without stubs. It is shown that the signals around 1.25 GHz and 1.95 GHz are absorbed by the stubs.

Note that the measured S-parameters here include the SMA connectors as well as the on-board patterns, however, the effects of the SMA connectors are small compared with the effects of the patterns, and the SMA connectors are included in both with/without stubs measurements, and hence the  $S_{21}$  difference reveals the characteristics of the stubs.



**Fig.5** Setup for the S parameter measurement. (a) without stubs, (b) with stubs.

#### 4.2 Spectra

Figure 7 shows the measured spectrum of the power supply noise of the repeat mode at the 1.25 GHz operation with/without the stubs. This graph shows that the dominant noise frequency is the operating frequency, and the stub eliminates the 1.25 GHz noise component. The spectrum of the random mode are shown in Fig. 8(i). Even though the noise is spread around the operating frequency because of its PRBS pattern, the stub suppresses the noise peak around 1.25 GHz.

The measured waveforms of the Vddn island on the random mode is shown in Fig. 9. It is also shown that the power supply noise is reduced by the stub. However, the noise of the random mode cannot be completely suppressed because of the lower frequency component which the stubs cannot suppress, as shown in Fig. 8.

## 4.3 Operating Frequency Dependence

The operating frequency dependence of the measured spectrum of the random mode is shown in Fig. 10. When the operating frequency and the stub frequency match in (i) and (iv), the spectrum have different peak amplitudes for with/without stubs. When the operating frequency does not match with the stub frequency, the spectrum are similar for with/without stubs. Figure 11(a) shows the operating frequency dependence of the noise amplitude of the operating







**Fig.7** Measured spectrum of the repeat mode at 1.25 GHz operation of the with/without stubs cases.



**Fig.8** Measured spectrum of the random mode at 1.25 GHz operation of the with/without stubs cases. (i-b) The spectrum of the lower frequency.



**Fig.9** Measured power supply noise waveform of the random mode at 1.25 GHz operation of the with/without stubs cases.

frequency component, and Fig. 11(b) shows the operating frequency dependence of the total noise, with the line of the (i)–(v) frequencies. The total noise value here is defined by the standard deviation  $\sigma$  from the average voltage  $V_{av}$ ,

$$V_{av} = \frac{1}{N} \sum_{i=1}^{N} V_i, \quad \sigma = \sqrt{\frac{1}{N-1} \sum_{i=1}^{N} (V_i - V_{av})^2}$$
(6)

where N is the number of the sampling points which is 4096, and the sampling time step is constant in this experiment, as shown in Fig. 9.

The graph (a) indicates that the stubs for 1.25 GHz, 1.95 GHz remove 87%, 72% of the designed frequency noise, in case (i), (iv), respectively. The total noise reduction ratio of with/without stubs are 39% in case (i) and 19% in case (iv), as shown in Fig. 11(b). The total noise reduction ratio by the stub is not as good as the reduction ratio



Fig. 10 Operating frequency dependence of the random mode spectrum.

of the operating frequency component because of the lower frequency components.

## 5. Discussion

#### 5.1 Lower Frequency Noise

As shown in Fig. 8(i-b), the power supply noise spectrum have some amount of power in lower frequency components. The PRBS  $2^7 - 1$  circuit generates pseudo-random bit pattern which repeats in every  $2^7 - 1 = 127$  clock cycles, and the stream has 1.25 GHz/127 = 9.84 MHz component as the basic frequency at the 1.25 GHz operation. Figure 8(i-b) shows that the lower frequency set are the harmonics of the basic frequency. It means that these noises are caused by the



Fig. 11 Operating frequency dependence of the power supply noise in random mode. (a) Noise amplitude of the operating frequency component. (b) Total noise amplitude.



Fig. 12 Current measurement using a magnetic probe.  $\circ$  and  $\Box$  indicate the measured points.

PRBS  $2^7 - 1$  stream characteristics.

## 5.2 Current Distribution along the Stubs

When a noise frequency matches with a stub frequency, the current and the voltage distribution along the stub are

$$|I(z)| = A\cos(\beta z), \quad |V(z)| = -jAZ_0\sin(\beta z) \tag{7}$$

where A is a constant value,  $\beta$  is the phase constant defined by Eq. (2) and z is the location of the stub.

The current distribution along the stubs are measured by using a magnetic probe [7] which picks up the magnetic field caused by the current and measures the induced voltage



**Fig. 13** Normalized current distribution along the stubs. The markers are measurement results, and the dashed lines are ideal curves given by Eq. (7).



Fig. 14 ITRS roadmap of MPU clock frequency, and corresponding stub length.

by the spectrum analyzer, as shown in Fig. 12. The current was measured at ten points for each stub when the operating frequency is 1.25 GHz/1.95 GHz for the 1.25 GHz/1.95 GHz stubs, respectively, and the results are shown in Fig. 13 with the ideal distribution given by Eq. (7). Since the magnetic probe has frequency dependence between the current and the induced voltage amplitude, the graph shows the normalized current value for each stub. The measured and theoretical current distribution have same tendency, showing that the stubs work for the power supply noise reduction of the designed frequency.

## 5.3 Operating Frequency Dependence

As being discussed in the previous section, the stubs remove the noise of the designed frequencies. In case (iii), however, the noise amplitude of the operating frequency is suppressed even though the frequency is not the frequencies of the stubs, as shown in Fig. 10(iii) and Fig. 11(a). It is likely caused by the package and bonding wire frequency characteristics. The transistor switchings occur inside the LSI package, and the impedance of the package and bonding wire is large enough at the frequency that the noise does not come out from the package. Thus, the noise of the frequency is not observed.

#### 5.4 Possibility for On-Chip Stubs

The stub length is in inverse proportion to the operating frequency, as being expressed by Eq. (4), and the dielectric constant becomes 3.9 if the stubs are integrated on-chips because the stubs stay in SiO<sub>2</sub>. Figure 14 shows the prediction of the required stub length based on the ITRS roadmap of MPU clock frequency [8]. It shows that the stub length will be shortened to about 5 mm in 2007, and on-chip stubs will be possible.

#### 6. Conclusion

We have demonstrated the power supply noise reduction using on-board stubs. A quarter-length stub attached to the power supply line of an LSI chip works as a band-eliminate filter, and suppresses the power supply noise of the designed frequency. The measurement results show that 87% of the designed frequency noise component and 39% of the total noise are reduced when the stubs are attached to the power supply area on the PCB board for a 1.25 GHz operating test chip which has a PRBS generator with inverter chains. These results show the possibility of the stub onchip integration which can eliminate the package and bonding wire parasitic impedance effects when the chip operating frequency becomes higher and the stub length becomes shorter.

## Acknowledgement

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Hitachi Ltd. and Dai Nippon Printing Corporation. This study was supported by Grant-in-Aid for JSPS Fellows of the Ministry of Education, Culture, Sports, Science and Technology.

#### References

- M. Badaroglu, K. Tiri, S. Donnay, P. Wambacq, I. Verbauwhede, G. Gielen, and H. De Man, "Clock tree optimization in synchronous CMOS digital circuits for substrate noise reduction using folding of supply current transients," Proc. ACM/IEEE Design Automation Conf., pp.399–404, June 2002.
- [2] K.Y. Chen, W.D. Brown, L.W. Schaper, S.S. Ang, and H.A. Naseem, "A study of the high frequency performance of thin film capacitors for electronic packaging," IEEE Trans. Adv. Packag., vol.23, no.2, pp.293–302, May 2000.
- [3] T. Nakura, M. Ikeda, and K. Asada, "Theoretical study of stubs for power line noise reduction," Proc. IEEE Custom Integrated Circuits Conference, pp.715–718, Sept. 2003.
- [4] T. Nakura, M. Ikeda, and K. Asada, "Stub vs. capacitor for power supply noise reduction," IEICE Trans. Electron., vol.E88-C, no.1, pp.125–132, Jan. 2005.
- [5] T. Nakura, M. Ikeda, and K. Asada, "Preliminary experiments for power supply noise reduction using stubs," Proc. IEEE Asia-Pacific Conf. on Advanced System Integrated Circuits, pp.286–289, Aug. 2004.

- [6] H. Johnson and M. Graham, High-Speed Digital Design, Appendix C, Prentice Hall PTR, 1993.
- [7] H. Wabuka, N. Matsuda, N. Tamaki, and H. Tohya, "Estimation of the RF current at IC power terminal by magnetic probe with multi-layer structure," Proc. IEICE EMCJ98-6, pp.39–43, April 1998.
- [8] "International technology roadmap for semiconductors 2002 update,"
   [Online] Available: http://public.itrs.net/



**Toru Nakura** was born in Fukuoka, Japan in 1972. He received the B.S. and M.S. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1995 and 1997 respectively. Then he worked as a high-speed communication circuit designer using SOI devices for two years, and worked as a EDA tool developer for three years. He joined the University of Tokyo again as a Ph.D. student in 2002. His current interest includes signal integrity on high-speed operation LSI circuits.



Makoto Ikeda received the B.S., M.S., and Ph.D. in electronics engineering from the University of Tokyo, Tokyo, Japan, in 1991, 1993, and 1996, respectively. He joined the Department of Electronic Engineering, the University of Tokyo as a Faculty Member in 1996, and is currently an Associate Professor at VLSI Design and Education Center, the University of Tokyo. His research interests includes the reliability of VLSI design. He is a member of the Institute of Electrical and Electronics Engineers (IEEE),

and the Information Processing Society of Japan (IPSJ).



Kunihiro Asada was born in Fukui, Japan, on June 16, 1952. He received the B.S., M.S., and Ph.D. in electronic engineering from the University of Tokyo in 1975, 1977, and 1980, respectively. In 1980 he joined the Faculty of Engineering, the University of Tokyo, and became a lecturer, an associate professor and a professor in 1981, 1985 and 1995, respectively. From 1985 to 1986 he stayed in Edinburgh the University as a visiting scholar supported by the British Council. From 1990 to 1992 he served as

the first Editor of English version of IEICE (Institute of Electronics, Information and Communication Engineers of Japan) Transactions on Electronics. In 1996, he established VDEC (VLSI Design and Education Center) with his colleagues in the University of Tokyo. It is a center supported by the Government to promote education and research of VLSI design in all the universities and colleges in Japan. He is currently in charge of the head of VDEC. His research interests are design and evaluation of integrated systems and component devices. He has published more than 400 technical papers in journals and conference proceedings. He has received Best Paper Awards from IEEJ (Institute of Electrical Engineers of Japan), IEICE and ICMTS1998/IEEE and so on. He is a member of the Institute of Electrical and Electronics Engineers (IEEE), and the Institute of Electrical Engineers of Japan (IEEJ).