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On-Chip *di/dt* Detector Circuit

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SUMMARY This paper demonstrates an on-chip di/dt detector circuit. The di/dt detector circuit consists of a power supply line, an underlying spiral inductor and an amplifier. The mutual inductor induces a di/dt proportional voltage, and the amplifier amplifies and outputs the value. The measurement results show that the di/dt detector output and the voltage difference between a resistor have good agreement. The di/dt reduction by a decoupling capacitor is also measured using the di/dt detector.

key words: *di/dt detector, mutual inductor, spiral inductor, parasitic inductance, power supply noise*

1. Introduction

As the process technology advances, the number of the transistors on an LSI chip has been increasing and their high speed operations generate more power supply noise while the low supply voltage reduces the noise margin. Thus, the power supply noise becomes a serious issue for the reliability of the LSI operations.

Recently, a di/dt noise is becoming one of the dominant source of the power supply noise along with an IR drop. An EMI noise also becomes a serious problem for high speed operating LSIs. Therefore, a current measurement technique, especially a high frequency di/dt measurement technique, is necessary in order to estimate the di/dt noise.

Many techniques have been proposed to measure the power supply voltage bounce [1]. On the other hand, only few techniques have been developed for the power supply current measurement. One technique uses a resistor connected in series to a power supply line on a PCB board and measures the voltage difference of the both terminals using electron-beam probing [2]. This technique needs numerical calculation to obtain the current and di/dt waveforms. Another technique picks up the magnetic field and measure the spectrum [3]. It is unable to reproduce the original current nor di/dt waveforms from the spectrum because the phase information is lost.

This paper demonstrates an on-chip di/dt detector circuit [4], [5]. According to the observed di/dt, this technique can be applicable to control the LSI system operations dynamically, such as operating frequency and power supply voltage control, because the detector is realized on-chip and outputs the di/dt value in real time.

In Sect. 2, the basic concept and the circuit design are presented. Section 3 analyzes and gives necessary equations of the di/dt detector. Measurement results and the applications are shown in Sects. 4 and 5, then Sect. 6 concludes this paper.

2. Circuit Design

2.1 Basic Concept

Figure 1 shows the block diagram of the di/dt detector circuit. A power supply current for the internal circuit goes through the power supply line inductance L_1. A pickup inductance L_2 coupled to L_1 with a coupling coefficient K induces a di/dt proportional voltage. A noise-tolerant amplifier amplifies the induced voltage and outputs to a $50\,\Omega$ transmission line that enables a high frequency measurement.

2.2 Mutual Inductor

The inductance L_1 should be small since it is in series connection to the power supply line. The small inductance requires a high coupling coefficient K and a bigger L_2 in order to generate the enough induced voltage on the terminal of L_2.

The mutual inductor consists of the power supply line and an underlying spiral inductor. The power supply line L_1 is composed of the top metal layer, ML3, with 1 turn, $20\,\mu$m width. The spiral inductor L_2 has 10 turns with $2\,\mu$m width and $2\,\mu$m spacing using ML1. The outside diameter of the both inductors are $140\,\mu\text{m} \times 140\,\mu\text{m}$, as shown in Fig. 2. This structure is called small mutual inductor. Another type of inductors, called large mutual inductor, has $200\,\mu$m diameter and 24 turns.

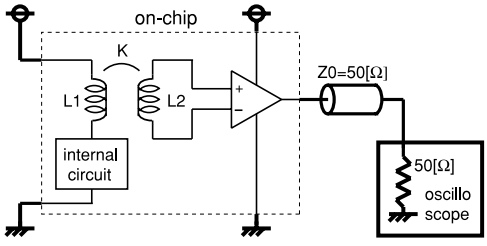

Fig. 1 Block diagram of the di/dt detector circuit. The bold lines represent outside devices.

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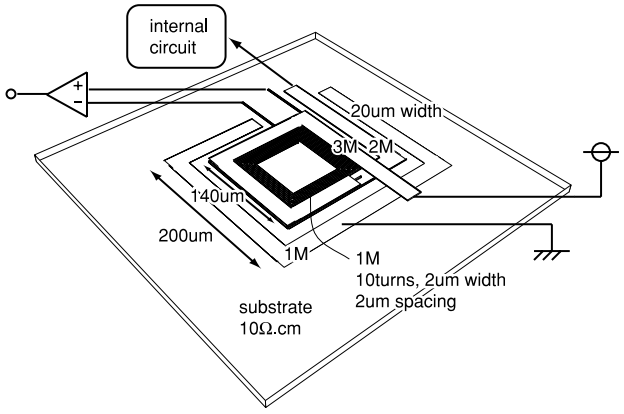

Fig. 2 Mutual inductor structure.

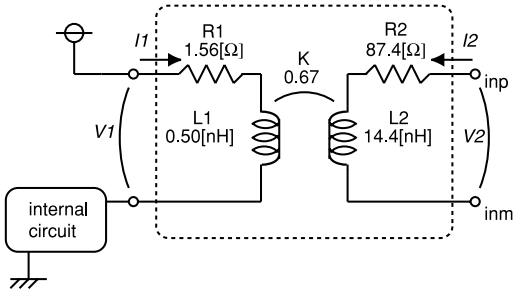

Fig. 3 Equivalent circuit of the small mutual inductor.

The equivalent circuit of this mutual inductor structure is extracted by FastHenry [6] as shown in Fig. 3.

2.3 Amplifier and Output Buffer

Since the output di/dt value is a high speed analog signal, a high frequency and high linearity amplification is the key issue for the amplifier design.

The amplifier schematic is shown in Fig. 4. We employ a current mirror type amplifier without current source. The resistors R_b are used to keep the DC bias voltage as half-vdd. The resistance is big enough to be considered open for AC signal. The bias condition realizes the maximum gain and the widest linearity for the amplifier.

We did not use a feedback type amplifier because it cannot respond to the high frequency signals. Moreover, the 50 Ω load is too small to keep the linearity of the amplifier gain even if the feedback amplifier is employed.

The output is connected to a transmission line whose characteristic impedance is 50 Ω. The blocking capacitor C_b is inserted at the input port of the oscilloscope to prevent the bias point change of the node $n2$ due to the 50 Ω termination resistor connected to GND.

Note that the average of di/dt value is zero because the current value is finite, so that the blocking capacitor does not affect the measurement.

According to HSPICE simulations, the gain of the amplifier G is 0.39, the cut-off frequency is 2.2 GHz when no load capacitance, and the output linearity range is about ±0.35 V, with the single amplifier structure.

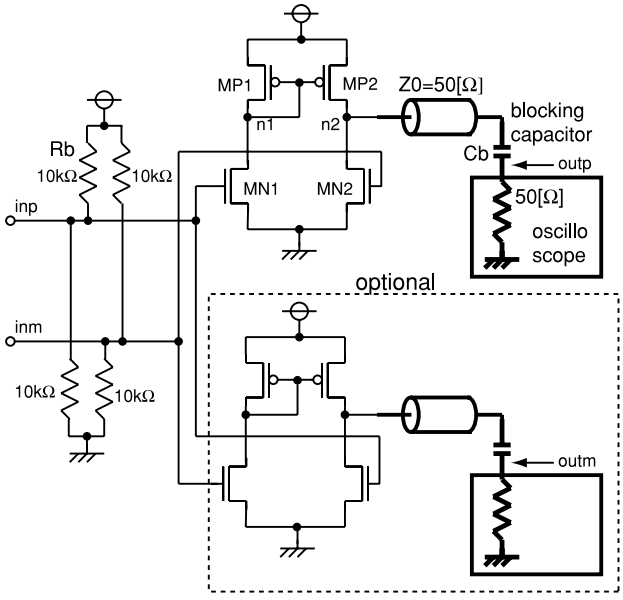

Fig. 4 Amplifier/Output buffer, and measurement setup.

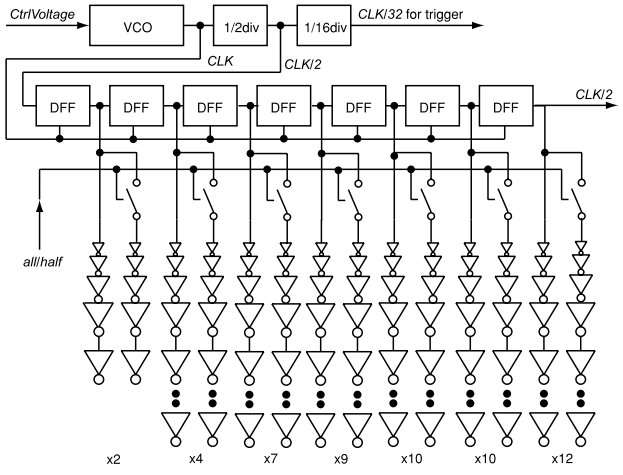

Fig. 5 Internal circuit.

Though the single amplifier structure is employed here because the characteristics of the amplifier is enough for our purpose, it can be improved by using the dual amplifiers with plus-minus exchanged inputs and measure the difference of the output, as shown in Fig. 4 "optional." We can eliminate asymmetric characteristics and unexpected common-mode noises, and also increase the linear operation range and the gain, with this structure.

2.4 Internal Circuit for Noise Source

The internal circuit is shown in Fig. 5. *CtrlVoltage* changes the operating frequency through the VCO. The 1/2 divider and the 1/16 divider generate $CLK/2$ signal which is the input for the DFF chain, and $CLK/32$ signal which is used

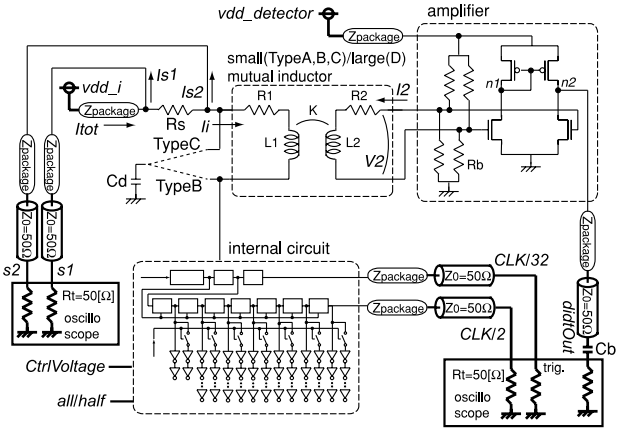

Fig. 6 Over-all circuit with the measurement setup.

as a trigger for the oscilloscope. Each DFF has an inverter chain whose switchings are the source of the di/dt. The length of the inverter chains are distributed from 2 to 12. The delay of the longest inverter chain is 0.625 ns. $all/half$ signal controls the activation ratio of the circuit.

2.5 Power Supply Line Structures

The power supply line has an on-chip resistor R_s in series, the both terminals of which are connected to output pins to enable the current measurement by calculating the voltage difference, and compare the result with the di/dt detector output as a reference. As shown in Fig. 6, the internal current goes out from *vdd_i* to the internal circuit through the package and bonding wire impedance $Z_{package}$, the series resistor R_s, and the inductor L_1.

Four types of circuits were designed. TypeA: no decoupling capacitor with the small mutual inductor, TypeB: the on-chip decoupling capacitor C_d at the node after the detector with the small mutual inductor, TypeC: the on-chip decoupling capacitor at the node before the detector with the small mutual inductor, TypeD: no decoupling capacitor with the large mutual inductor.

2.6 Overview and Measurement Setup

The internal circuit switching causes the di/dt which induces the voltage at the spiral inductor L_2 by the inductive coupling K. The amplifier amplifies and outputs the voltage to *didtOut*. The both terminals of the series resistor R_s are connected to the oscilloscope as $s1$, $s2$ signals. Since the input voltage $CtrlVoltage$ and $all/half$ are DC signals, no need to care the high-speed characteristics for them. $CLK/2$ and $CLK/32$ signals come out through output buffers whose supply voltage is *vdd_io* which is neglected in the figure for simplicity. $CLK/2$ signal is used to check if the circuit works fine, $CLK/32$ is used as a trigger for the oscilloscope.

3. Analytical Model

3.1 Equations

The mutual inductance M is

$$M = K\sqrt{L_1 L_2}. \tag{1}$$

Assuming that the input current of the amplifier is I_2, the output voltage of the mutual inductor V_2 is

$$V_2 = M\frac{dI_i}{dt} + R_2 I_2 + L_2\frac{dI_2}{dt} \approx M\frac{dI_i}{dt}. \tag{2}$$

Here I_2 is small enough because the input impedance is large enough compared with R_2 and ωL_2 ($\omega \ll 10\,\mathrm{GHz}$).

Assuming that the gain of the amplifier is G, the output voltage $V_{didtOut}$ of the di/dt detector circuit is

$$V_{didtOut} = GV_2 = GK\sqrt{L_1 L_2}\frac{dI_i}{dt} \tag{3}$$

which means

$$\frac{dI_i}{dt} = \frac{1}{GK\sqrt{L_1 L_2}}V_{didtOut} \equiv A_{v2didt}V_{didtOut} \tag{4}$$

where

$$A_{v2didt} \equiv \frac{1}{GK\sqrt{L_1 L_2}}. \tag{5}$$

Integrating Eq. (4) with respect to time,

$$I_i = A_{v2didt}\int V_{didtOut}dt + C. \tag{6}$$

The relation between the internal current I_i and the voltage of $s1$, $s2$ is

$$V_{s1} - V_{s2} = R_s(I_i + I_{s2}) \tag{7}$$

and this equation can be converted to

$$V_{s1} - \left(1 + \frac{R_s}{R_t}\right)V_{s2} = R_s I_i \tag{8}$$

using $I_s = V_s/R_t$, where R_t is the termination resistance 50 Ω. From Eqs. (6) and (8),

$$V_{s1} - \left(1 + \frac{R_s}{R_t}\right)V_{s2} = R_s A_{v2didt}\int V_{didtOut}dt + C. \tag{9}$$

Differentiate Eq. (9) by time,

$$V_{didtOut} = \frac{1}{R_s A_{v2didt}}\frac{d\{V_{s1} - (1 + R_s/R_t)V_{s2}\}}{dt}. \tag{10}$$

The detectable di/dt range and frequency are decided by the amplifier output linearity range and its frequency characteristics,

$$\left.\frac{dI_i}{dt}\right|_{range} = A_{v2didt}V_{amp\_outRange\_lin} \tag{11}$$

and the resolution of the detectable di/dt is decided by the resolution of the di/dt detector output voltage,

$$\left.\frac{dI_i}{dt}\right|_{res} = A_{v2didt}V_{didtOut\_res} \tag{12}$$

Table 1 Designed parameter value.

	L_1	L_2	K	G	A_{v2didt}	R_s
small	0.50 nH	14.4 nH	0.67	0.39	1.43 $(\text{nH})^{-1}$	1 Ω
large	0.86 nH	53.3 nH	0.60	0.39	0.63 $(\text{nH})^{-1}$	1 Ω

3.2 Designed Parameters

The series resistor R_s on the power supply line is formed using gate-poly with silicide, and the designed resistance value is about 1 Ω. The decoupling capacitor C_d is formed using poly-poly capacitor, and the designed value is about 700 pF. The bias resistor R_b is formed using gate-poly without silicide and the designed value is about 10 kΩ. The necessary parameter values are listed in Table 1.

4. Measurement Results

4.1 Setup

The chip was designed and fabricated using 0.35 μm 2-Poly 3-ML standard CMOS technology. The chip size is 4.9 mm × 4.9 mm and the chip photograph is shown in Fig. 7.

4.2 Sensitivity of the di/dt Detector

Figure 8 shows the waveforms of (a) $CLK/2$, (b) $s1$ and $s2$, (c) $V_{s1} - (1 + R_s/R_t)V_{s2}$ signal and the numerical-time-integral of the di/dt detector output multiplied by R_sA_{v2didt}, based on Eq. (9), (d) the di/dt detector output and the numerical-time-differential of $V_{s1} - (1 + R_s/R_t)V_{s2}$ signal divided by R_sA_{v2didt}, based on Eq. (10), of TypeA circuit. Since the $V_{s1} - (1 + R_s/R_t)V_{s2}$ waveform is noisy, we applied a smoothing before the numerical differentiation.

These graphs show that the currents measured by the series resistor voltage difference and the di/dt detector output have good agreement, and our di/dt detector circuit works well.

4.3 Accuracy of the di/dt Detector

The series resistance value R_s can be estimated from $s1$ and $s2$ voltage difference as shown in Fig. 8(b). Since the internal circuit does not consume current because of no switching at the arrows, the DC current going through the series resistor is the same as the current going into the termination resistor R_t of $s2$, and $I_{s2} = V_{s2}/R_t$. The series resistance value is $R_s = \Delta V/I_{s2} = R_t\Delta V/V_{s2} = 50 \times (3.20999 - 3.16070)/3.16070 = 0.78\,\Omega$. The designed value R_s=1 Ω is a rough estimation, and the measured value 0.78 Ω is reasonable.

The current value shown in Fig. 8(c) vertical axis is calculated using R_s=0.78 Ω, and the di/dt value in Fig. 8(d) vertical axis is calculated using A_{v2didt}=1.43 × 10^9. The error between the solid lines and the dashed lines in Figs. 8(c) and (d) are evaluated by the standard deviation,

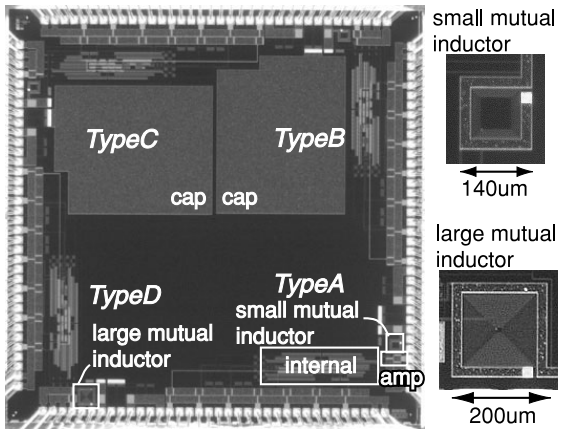

Fig. 7 Chip photograph. The chip size is 4.9 mm × 4.9 mm.

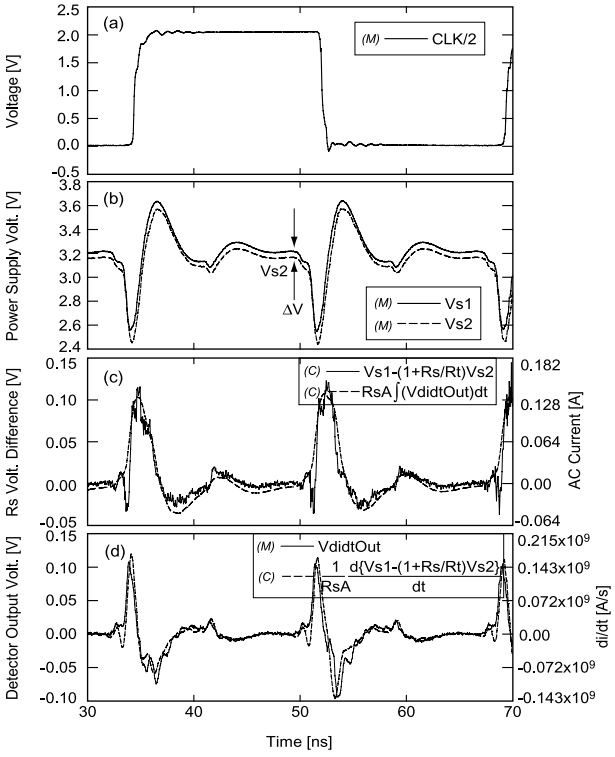

Fig. 8 Waveforms of (a) $CLK/2$, (b) $s1$ and $s2$, (c) $V_{s1} - (1 + R_s/R_t)V_{s2}$ signal and the numerical-time-integral of the di/dt detector output multiplied by R_sA_{v2didt}, based on Eq. (9), (d) the di/dt detector output and the numerical-time-differential of $V_{s1} - (1 + R_s/R_t)V_{s2}$ divided by R_sA_{v2didt}, based on Eq. (10), of TypeA circuit. The (M) and (C) in the signal caption represent the measured and calculated waveforms, respectively. The current and di/dt values on the right vertical axis in the graph (c) and (d) are calculated using R_s=0.78 Ω and A_{v2didt}=1.43 × 10^9, respectively.

$$\sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(V_{solid} - V_{dashed})^2} \tag{13}$$

from 30 ns to 65 ns region and the number of the sampling points N is about 700. The error in the graph (c) is σ=4.49 mV which corresponds to 5.8 mA, and the error in the graph (d) is σ=4.38 mV which corresponds to

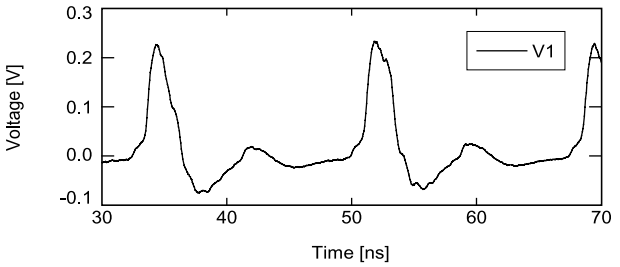

Fig. 9 HSPICE simulation waveform of the voltage drop between the detector terminals V_1 using the impedance shown in Fig. 3 and the current waveform shown in Fig. 8(c) dashed line.

6.3×10^9 mA/s.

4.4 Input Impedance of the di/dt Detector

The primary part L_1 and R_1 of the mutual inductor is inserted in series to the power supply line, and the impedance disturbs the power supply voltage for the internal circuit. Figure 9 shows the HSPICE simulation waveform of the voltage drop between the detector terminals V_1 using the impedance shown in Fig. 3 and the current waveform shown in Fig. 8(c) dashed line.

Since this is a feasibility experiment, we employ a conservative design on the mutual inductor structure and the peak voltage drop is from −0.1 V to 0.2 V. However, the voltage can be reduced with smaller resistance R_1 and inductance L_1 on the power supply line by using a thicker metal, multi-layer (ML2 and ML3 together, for example), wider power supply line or a straight power supply line with a adjacent spiral inductor if lower sensitivity is acceptable.

5. Applications

5.1 Decoupling Capacitor Effects

Figure 10 shows the measured waveforms of (a) $s1$, and (b) the di/dt detector output, of TypeA, B, C circuits. The decoupling capacitors of TypeB, C provide AC currents to the internal circuits and the di/dt magnitude in the current through the package parasitic inductance is reduced considerably so that the power supply voltage bounce are suppressed as shown in Fig. 10(a).

The decoupling capacitor on TypeB circuit suppresses the AC current going through the di/dt detector so that the di/dt detector output voltage is small, as shown in Fig. 10(b). The decoupling capacitor on TypeC circuit provides bigger and sharper AC current to the di/dt detector compared with the no decoupling capacitor circuit of TypeA. This is because the impedance $Z_{package}$ on the power supply line of TypeA works as a current regulator for AC components, while the decoupling capacitor of TypeC works as a constant voltage source.

5.2 Activation Ratio, Mutual Inductance Dependency

The measured waveforms of $s1$ and the di/dt detector output

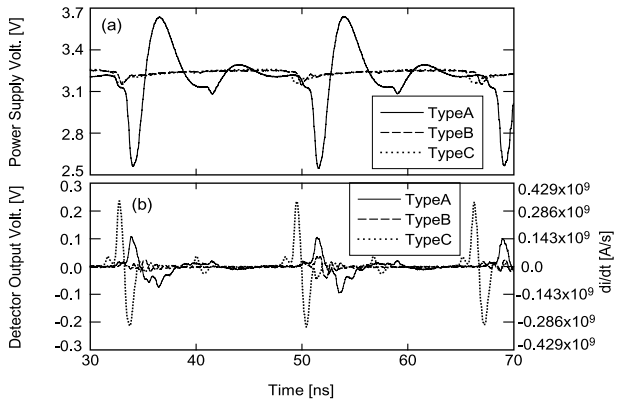

Fig. 10 Measured waveforms of (a) $s1$, and (b) the di/dt detector output, of TypeA, B, C circuits.

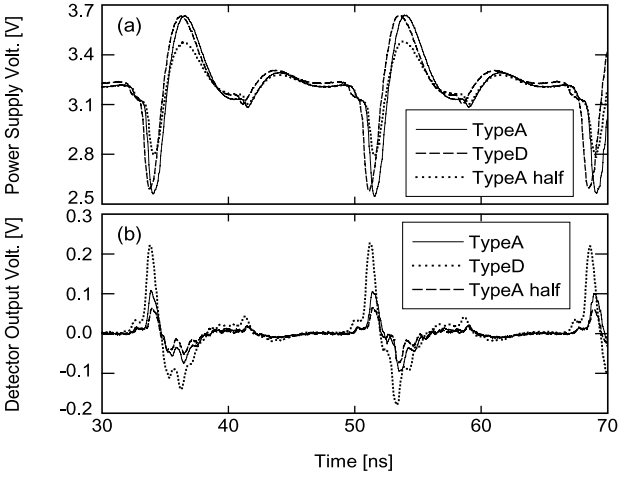

Fig. 11 Measured waveforms of (a) $s1$, and (b) the di/dt detector output voltage, of TypeA, TypeD, and TypeA of the half activation ratio.

voltage of TypeA, TypeD, and TypeA of the half activation ratio, are shown in Figs. 11(a) and (b). The graph (a) shows that the power supply voltage bounce of TypeA and TypeD circuits are almost the same. This is due to the same internal circuits and the same parasitics of the package $Z_{package}$, while the L_1 difference makes the small difference on the waveforms. The half activation case has the half di/dt of the internal circuit, thus the smaller voltage bounce. The voltage bounce is not a half because of the parasitic capacitance of the internal circuit, the pads, the package and so on.

As for the di/dt detector output waveforms of the Fig. 11(b), the waveform of TypeD circuit has almost the same shape with about $A_{v2didt\_large}/A_{v2didt\_small}$=2.27 times magnitude compared with the waveform of TypeA circuit. On the half activation ratio case, the di/dt detector output has about a half magnitude with the same shape.

These results also confirm the di/dt detector performance.

6. Conclusion

The on-chip di/dt detector circuit has been demonstrated. Our di/dt detector circuit consists of a power supply line, an underlying spiral inductor and an amplifier. The mutual inductor induces a di/dt proportional voltage, and the amplifier amplifies and outputs the value. The measurement results show that the di/dt detector output and the voltage difference between a resistor have good agreement with the accuracy of 6.3×10^9 mA/s. The current waveform can be obtained with the accuracy of 5.8 mA by integrating the di/dt waveform. The di/dt detector also detects the decoupling capacitor effects for the di/dt reduction. Since on-chip and real-time di/dt measurements are possible, our di/dt detector circuit can be applicable for feedback di/dt control as well.

Acknowledgement

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