Feedforward Active Substrate Noise Cancelling Technique using Power Supply di/dt Detector

Toru Nakura†, Makoto Ikeda‡, and Kunihiro Asada‡
†Dept. of Electronic Engineering, ‡VLSI Design and Education Center (VDEC), †,‡University of Tokyo, Tokyo, Japan
{nakura, ikeda, asada}@silicon.t.u-tokyo.ac.jp

Abstract — This paper demonstrates a feedforward active substrate noise cancelling technique using a power supply di/dt detector. Since the substrate is tied to the ground line, the substrate noise is closely related to the ground bounce which is caused by di/dt when inductance is dominant on the ground line impedance. Our active cancelling technique detects the di/dt of the power supply current and injects an anti-phase signal into the substrate so that the di/dt proportional substrate noise is cancelled out. 34% of the substrate noise reduction was achieved in a test circuit for our first trial. It is theoretically shown that the optimized canceller design will enhance the suppression ratio up to 56%.

keywords: substrate noise, feedforward active cancelling, anti-phase, ground bounce, di/dt detector

Introduction

As the growing demand of analog-digital mixed signal LSIs such as A/D, D/A and PLL integrated with large scale digital circuits, substrate noise becomes serious concern. Although power lines for digital and analog circuits are isolated in order to prevent the coupling of the digital switching noise to the analog circuits, the digital switching noise is transferred to the analog blocks via the common substrate.

Noise on a power line is caused by di/dt noise and resistive voltage drops due to the parasitic impedance of the power line. Typically, the digital ground line is connected to the substrate in every CMOS gate, which results in a very low resistance between the digital ground line and the substrate, and hence the digital ground noise and ringing will also be present on the substrate. One report shows that the substrate noise has the same shape with 1/8 amplitude of the ground noise[1].

Guard rings are widely used to suppress the substrate noise. However, the parasitic impedance of the guard line degrades the efficiency of the noise absorption especially for high frequency noise[2]. Another method is a feedback active guard band filtering[2][3]. The anti-phase noise signal is actively supplied to the guard band so that the original substrate noise is cancelled out. In this technique, an amplifier is used to sense the original substrate noise and generates the anti-phase noise signal. However, the frequency response and the delay of the amplifier restricts the bandwidth of the cancellable noise, so that the noise reduction ratio is not enough for practical applications. And feedback systems are sometimes unstable.

This paper demonstrates a feedforward active substrate noise cancelling technique using a power supply di/dt detector.

Circuit Design

A. Substrate Noise and di/dt

The main cause of substrate noise is a coupling from digital power lines. Ground noise is caused by the supply current and the ground line impedance. The ground noise amplitude is proportional to the di/dt if inductance is dominant in the ground line impedance. Therefore, the substrate noise is also proportional to the di/dt. Here, a di/dt detector[4] can be applicable for cancelling the di/dt proportional substrate noise.

A block diagram of our feedforward active substrate noise cancelling system is shown in Fig.1. The ground noise is caused by the power supply di/dt and L_{gnd}. The ground noise is transferred to the analog circuit through the substrate resistance. The p-sub/Nwell junction capacitor is negligibly small compared with the ground line-substrate impedance that the Vdd_D bounce is not transferred to the substrate. Since the substrate noise is proportional to the di/dt, the di/dt detector inverted output has anti-phase against the substrate noise. If the anti-phase signal is injected into the substrate, it can cancel the original substrate noise.

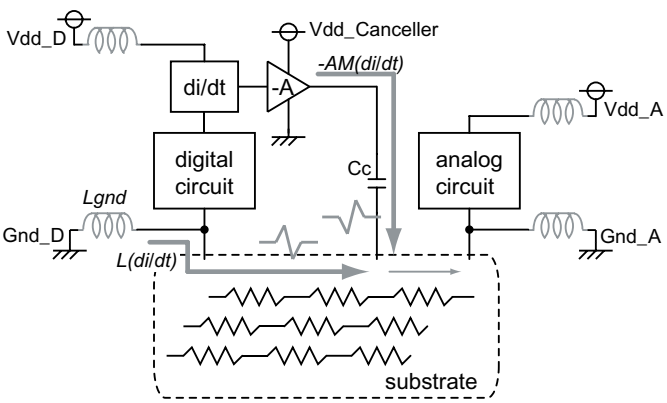

Fig. 1. Feedforward active substrate noise cancelling.

B. Noise Canceller

The substrate noise canceller is basically the same as the di/dt detector[4], where a mutual inductor coupled to the power supply line induces the di/dt proportional voltage, and an amplifier amplifies and outputs the value. The difference of the noise canceller here is that the plus-minus terminals of the amplifier inputs from the mutual inductor are exchanged in order to generate the "anti"-phase signal, as shown in Fig.2.

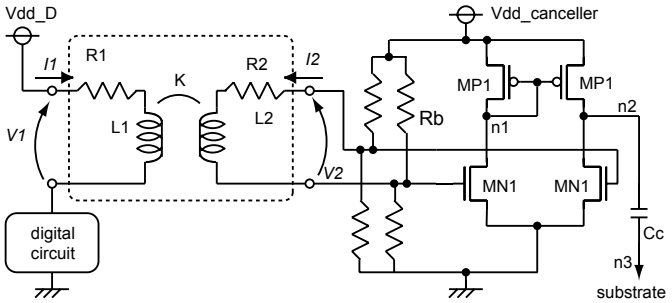

Fig. 2. Active substrate noise canceller.

Since the substrate is tied to the ground voltage, the coupling capacitor C_c is inserted at the output of the amplifier to prevent the bias voltage change of the node $n2$.

Here, the input impedance of the substrate from the injection point is assumed to be pure resistive. In order to inject the current with the appropriate phase, the impedance of the coupling capacitor C_c should be small enough compared with the substrate resistor impedance. Then, the amplifier can be considered as a voltage controlled current source. Therefore, the injected current has the same phase as $-V2$ which has the anti-phase against the di/dt.

C. Substrate Noise Probing for Verification

The substrate noise probing circuit implemented for verification purpose is shown in Fig.3. The noise is probed using an differential amplifier at the first stage with one input connected to the substrate and the other to an external ground as a reference. The input terminals are biased as half-Vdd by the resistors R_b, where the amplifier has the maximum gain. The resistance is large enough to be considered as open for AC signals. Since the substrate voltage is around ground voltage, the coupling capacitors C_c are used here as well. The second and the third stage amplifiers are composed of PMOS and resistors, and the final stage is a PMOS open drain structure.

Since substrate contacts of NMOS may change the substrate noise waveform, the body terminals of MN1 in the amplifier are not tied even though it may lead to an unstable amplifier operation. The second and third stage amplifiers are composed without NMOS to eliminate the substrate contacts. Here, the ratio of $\Delta I_d/\Delta V_g$ and $\Delta I_d/\Delta V_{bs}$, which is g_m/g_{bs}, is 6.0 according to HSPICE simulation. Thus, the amplifier has enough gain even though the noise voltage for the gate and the substrate are the same.

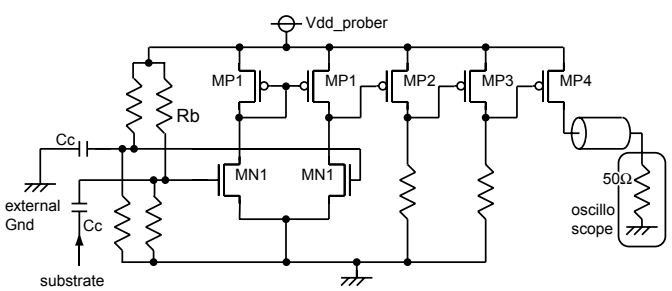

Fig. 3. Substrate noise prober.

D. Internal Circuit as Noise Source

Figure 4 shows our internal circuit as a noise generator. The test circuit contains VCO so that we can easily sweep the operating frequency by changing the DC control voltage ($Vctrl$). The frequency divider generates 101010... signal for the input to the shift resister. The SEL circuit can select the operating mode, a repeat mode or a random mode. On the repeat mode, the SEL circuit always outputs "High" signal, the signal change from the DFFs are transferred to the inverter chains and the circuit consumes the same amount of current at every clock cycle. On the random mode, the SEL circuit passes $CLK/4$, $CLK/8$ signals, the DFF outputs and some inverter chains are disconnected when the SEL outputs are "Low", and hence the current waveform becomes different in accordance with the divided clock signals. $allORhalf$ signal controls the activation ratio of the circuit. The $CLK/32$ output is used as a trigger for a oscilloscope, and the $CLK/2$ output is used as a reference for the timing consideration.

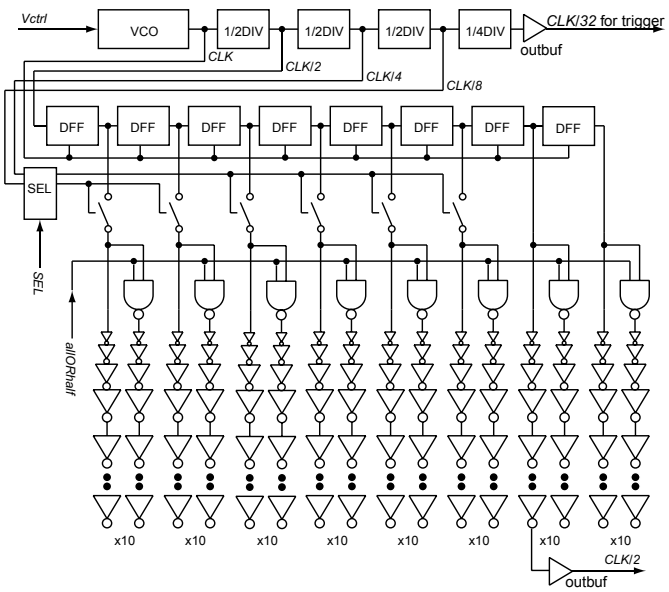

Fig. 4. Internal circuit as a noise source.

E. Design Parameters

The circuit is designed using 0.35μm 3-ML 2-Poly standard CMOS technology. The mutual inductor of the di/dt detector consists of the power supply line and an underlying spiral inductor. The power supply line L_1 is composed of the top metal layer ML3 with 1 turn, 20μm width. The spiral inductor L_2 has 24 turns with 2μm width and 2μm spacing using ML1. The outside diameter of the both inductors are 200μm $\times$ 200μm. The equivalent circuit of this mutual inductor structure is extracted by FastHenry 3D field solver. The coupling capacitor C_c is formed using poly-poly capacitor, and the designed value is about 25pF. The bias resistor R_b is formed using gate-poly without silicide and the designed value is about 10kΩ. The necessary parameter values are listed in Table I.

TABLE I
Designed Parameter Value

mutual inductor	L_1	L_2	K	R_1	R_2
	0.86nH	53.3nH	0.603	2.3Ω	218Ω
amp for canceller	W_{pmos}	W_{nmos}	R_b	C_c	
	200μm	100μm	10kΩ	25pF	
amp for prober	W_{pmos1}	W_{nmos1}	R_b	C_c	W_{pmos4}
	20μm	10μm	10kΩ	25pF	160μm

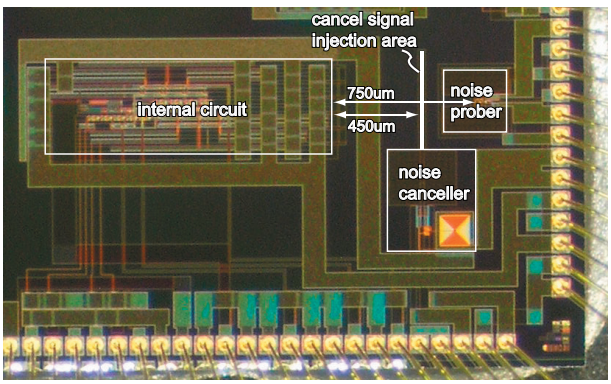

Fig. 5. Chip photograph of the feedforward active noise cancelling circuit, using 0.35μm CMOS process. The area is 3.0mm×1.8mm.

F. Floorplan

Figure 5 shows a chip photograph of our test circuit. The chip area is 3.0mm×1.8mm.

The substrate noise probing point is located 750μm apart from the noise source, and the cancel signal injection area is located between the noise source and the probing point.

Measurement

A. Setups

In order to measure high-speed noise waveforms, the chip is mounted on a Cu board as shown in Fig.6. All the inputs including *Vdd_internal*, *Vdd_io*, *Vdd_canceller*, *Vdd_prober*, *Vctrl*, *SEL* and *allORhalf* are DC and supplied through lead lines to the "islands" on the board. The voltage of the islands are stabilized by several chip capacitors. 50Ω transmission lines are directly connected to the high-speed output pins including *CLK*/2, *CLK*/32 and the substrate noise prober output, in order to reduce reflections.

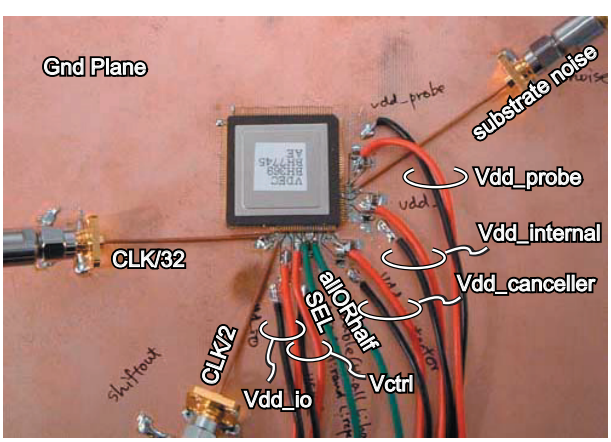

Fig. 6. Photograph of the chip mount.

B. Substrate Noise Waveforms

The measured waveforms of the substrate noise and the *CLK*/2 signals are shown in Fig.7. The active cancel OFF/ON means *Vdd_canceller*=0V/3.3V. Figure 7(a) is on the repeat mode, and Fig.7(b) is on the random mode. The operating frequency is 500MHz, and the gain of the noise prober at this frequency is about 7.5 by HSPICE simulation. The prober output has about 1V bias because the on-resistance of the final stage PMOS of the prober circuit is about 100Ω, as shown in Fig.3. The graphs show that our feedforward active cancelling circuit cancels and reduces the substrate noise of 30% on the repeat mode and 24% on the random mode if the peak-to-peak voltages are concerned.

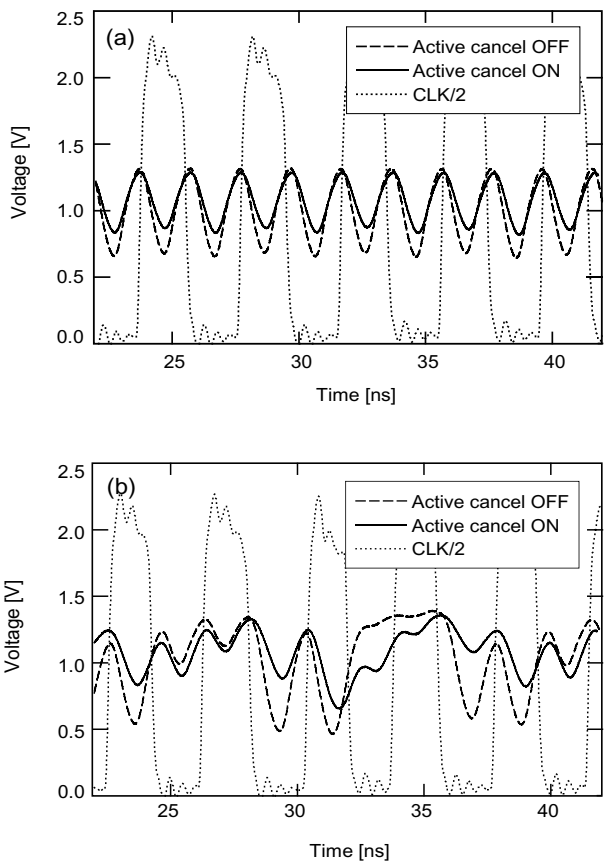

Fig. 7. Substrate noise waveforms with the active noise cancelling ON/OFF, together with the *CLK*/2 signal. The operating frequency is 500MHz. (a) Repeat mode, and (b) Random mode.

C. Frequency Dependence

The frequency dependence of the upper and lower peaks of the substrate noise voltage, together with its suppression ratio, on the repeat mode are shown in Fig.8. 17% to 34% of the substrate noise is suppressed from 100MHz to 600MHz operation range by our feedforward active noise cancelling circuit.

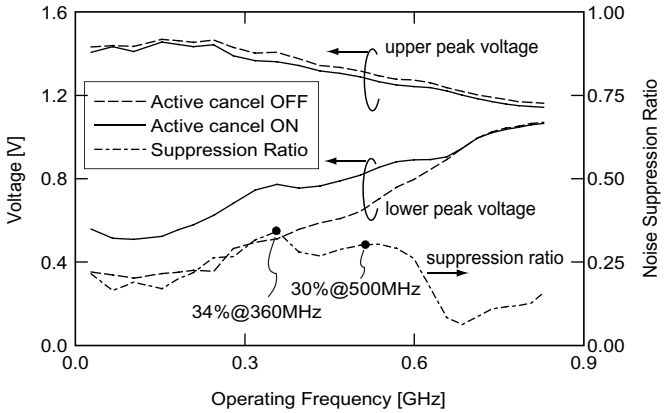

Fig. 8. The frequency dependence of the upper and lower peaks of the substrate noise voltage, together with its suppression ratio by the feedforward active noise cancelling, on the repeat mode.

Discussion

A. Current Injection

The amplitude of the injected current for the noise cancelling is controlled by the noise canceller supply voltage *Vdd_canceller*, and *Vdd_canceller* dependence of the substrate noise is shown in Fig.9(a). The graph shows the upper and lower peak voltage change at 500MHz operation on the repeat mode. It is shown that the substrate noise starts to be reduced around 1.0V as the cancelling signal increases until being saturated around 2.5V. It is because the noise injection amplifier starts to operate over 1.0V, and its gain is saturated around 2.5V because the transconductance g_m of MP1 and MN1 saturates.

The phase and amplitude of the substrate noise is plotted in a phasor diagram as shown in Fig.9(b). The phase is relative to $CLK/2$. The trace of the phasor with *Vdd_canceller* sweeping from 0V to 3.3V by 0.1V step shows that the phase of the injected current in this graph is $-\pi/2$. It also shows that more current injection by using bigger transistor width for MP1 and MN1 of the canceller amplifier will suppress more substrate noise. The minimum substrate noise by using the optimum MP1 and MN1 is V_{min} in Fig.9(b), and the optimum noise suppression ratio is 56%. V_{min} depends on the phase difference between the substrate noise and the di/dt. If the phase of the substrate noise and di/dt completely match (i.e. θ=0), V_{min} could be zero.

The anti-phase current is injected to cancel the substrate noise here. Another type of injection circuit, whose plus-minus terminals of the amplifier inputs are exchanged to realize "in"-phase current injection, has been implemented for a reference. Other circuits are exactly the same and the chip photograph looks the same as Fig.5. The in-phase current injection increases the substrate noise as shown in Fig.9(a) dashed line. It supports the model that the substrate noise reduction in the previous section is realized by our feedforward active cancelling scheme, not by other reasons. The cause of the substrate noise difference between the anti-phase and the in-phase at *Vdd_canceller*=0 in Fig.9(a) is considered as the process variation. Since the test chips of the anti-phase injection and the in-phase injection are different, the offsets and gains of the noise canceller and the noise prober have different characteristics in each chip.

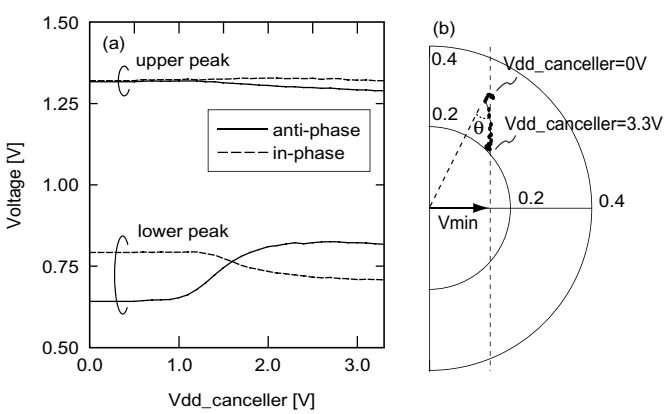

Fig. 9. (a) Noise canceller supply voltage dependence of the substrate noise amplitude, and (b) Phasor of the substrate noise, sweeping *Vdd_canceller*=0V to 3.3V by 0.1V step, on the repeat mode at 500MHz operation.

Summary

A feedforward active substrate noise cancelling scheme has been demonstrated. Our active cancelling technique detects the di/dt of the power supply current and injects an anti-phase signal into the substrate so that the di/dt proportional substrate noise is cancelled out. 30% of the substrate noise reduction was achieved in our 500MHz operating test circuit, and 17% to 34% of the substrate noise reduction is observed from 100MHz to 600MHz range. The substrate noise phasor measurement result shows that the optimum transistor width of the current injection amplifier will enhance the noise suppression ratio up to 56%.

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