Preliminary Experiments for Power Supply Noise Reduction using Stubs

Toru Nakura, Makoto Ikeda*, and Kunihiro Asada*
Dept. of Electronic Engineering, *VLSI Design and Education Center (VDEC),
Univ. of Tokyo, Tokyo 113-8656, Japan
{nakura, ikeda, asada}@silicon.t.u-tokyo.ac.jp

Abstract — This paper demonstrates a power supply noise reduction using stubs. A quarter-length stub attached to the power supply line of an LSI chip works as a band-eliminate filter, and suppresses the power supply noise of the designed frequency. Preliminary experiments show that 90% of the designed frequency noise component is suppressed when off-chip stubs are attached to a power supply pin of a 1.15GHz operating LSI. The results show the possibility of the stub on-chip integration when the operating frequency of LSIs becomes higher and the stub length becomes shorter.

Introduction

As the process technology advances, the number of the transistors on a LSI chip has been increasing and their high speed operations generate more power supply noise while the low supply voltage reduces the noise margin. Thus, the power supply noise becomes a serious issue for the reliability of the LSI operations.

Recently, a di/dt noise is becoming one of the dominant source of the power supply noise along with an IR drop. An EMI noise caused by the di/dt also becomes a serious problem for high speed operating LSIs. In order to suppress the di/dt, some methods, such as a semi-asynchronous architecture[1] and an inserting decoupling capacitor method[2] have been proposed. However, these methods make the circuit design complex and difficult, and an on-chip decoupling capacitor requires more die area, an off-chip decoupling capacitor does not work well due to the parasitic inductance on the terminal.

We have proposed the basic concept of using stubs for power supply di/dt reduction[3], where the simulation results show that the stub attached to the power supply line of an LSI chip reduces the power supply noise caused by the di/dt, and the stub will work more efficiently as the operating frequency of LSIs becomes higher. The focus of this paper is the experimental results of the stub di/dt reduction.

Theorem

As the operation frequency becomes higher and the wavelength of voltage and current gets comparatively smaller with the interconnect wire length, the wires should be considered as transmission lines instead of lumped RC elements. The characteristic impedance Z_0 and the phase constant β_c of the transmission lines are

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (1)$$

$$\beta_c = -j\sqrt{(R + j\omega L)(G + j\omega C)} \quad (2)$$

where R, L, G, C are the resistance, inductance, admittance representing the dielectric loss, capacitance of the wire, per unit length respectively.

The input impedance of the transmission line with its length l and the termination impedance Z_l is

$$Z_{stub} = Z_0 \frac{Z_l \cos\beta_c l + jZ_0 \sin\beta_c l}{Z_0 \cos\beta_c l + jZ_l \sin\beta_c l}. \quad (3)$$

When open termination (Z_l=∞), and if the transmission line has no loss ($R = G = 0$) and its length is quarter of the signal wavelength ($\beta_c l=\pi/2$), the input impedance of the stub becomes zero ($Z_{stub} = 0$), which is equivalent with infinite capacitance. When this stub is attached to the power supply line, the voltage fluctuation is suppressed.

The dominant frequency of the switching currents is the operating frequency f_0. Thus, the stub length adjusted for the operating frequency becomes

$$l = \frac{\pi/2}{\beta_{r0}} = \frac{\lambda_0}{4} = \frac{c/\sqrt{\epsilon_r}}{4f_0} \quad (4)$$

where λ_0, c and ϵ_r are the signal wavelength in the transmission line, the speed of light in vacuum and the dielectric constant.

Since the maximum operating frequency of our test chip is about 2GHz and the stub length becomes over 15mm in SiO_2, it is too long to realize the stub on-chip and we use off-chip stubs here as a preliminary experiment.

Setups

A. Test Circuit

A PRBS (Pseudo Random Bit Stream) $2^7 - 1$ generation circuit with an inverter chain at each output of the DFF is used as our test circuit, as shown in Fig.1. This circuit represents common synchronous circuits. The PRBS pattern and the inverter chains represent the random switching of LSIs and the combination logics, respectively. The length of the inverter chains distributes from 2 to 12, which represents a path length distribution between DFFs.

The test circuit contains VCO so that we can easily sweep the operating frequency by changing the DC control voltage (*vctrl*). The selector circuit selects the random mode which use the feedback from the XOR gate, and the repeat mode which use the $clk/2$ signal, to the input of the shift register. The repeat mode is the optimistic case and the random mode is the pessimistic case from the stub noise reduction point of view.

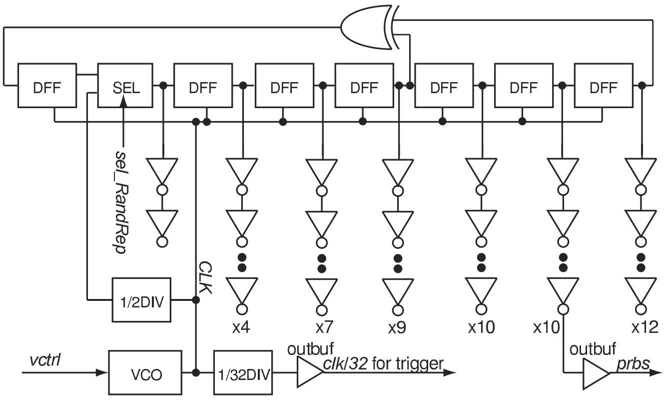

Fig. 1. Internal circuit. A PRBS generator and inverter chains. The *sel* signal selects the repeat mode or random mode.

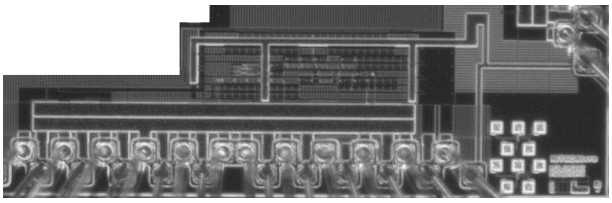

Fig. 2. Chip photograph. 0.18μm 5ML CMOS, 2mm×0.5mm.

The circuit is designed and fabricated using 0.18μm 5ML standard CMOS technology. The size of the test circuit is about 2mm×0.5mm.

B. Measurement Setup

The chip is mounted on Cu board as shown in Fig.3, and the corresponding schematic is shown in Fig.4. The DC bias of *vdd*, *vddio*, *vctrl* and *sel* are supplied through lead lines to the islands on the board. The voltage of the islands are stabilized by several chip capacitors. The *vddn* island which is the power supply for the internal circuit is connected to the *vdd* island by a wire and has no chip capacitor. The parasitic inductance of the wire causes noise voltage to the *vddn* island. The *vddn* island has two stubs. One is for 1.15GHz noise and the other is for 1.80GHz noise elimination. The voltage of the *vddn* island is probed by 50Ω transmission line so that the power supply noise can be measured by the spectrum analyzer and the oscilloscope. Other 50Ω transmission lines are also connected to the $clk/32$ and $prbs$ output pins of the test chip, and connected to the oscilloscope.

C. Stub Design

In this experiment, the stubs are adjusted for 1.15GHz and 1.80GHz whose stub length are 6.52cm and 4.17cm, respectively, according to eqn(4). The diameter of the stub is about 1mm. The one edge of the stub is soldered to the *vddn* island, and the rest of the part stay in the air with the height of about 1mm from the board. The stubs are easily removed so that we can compare the measurement results with/without the stubs.

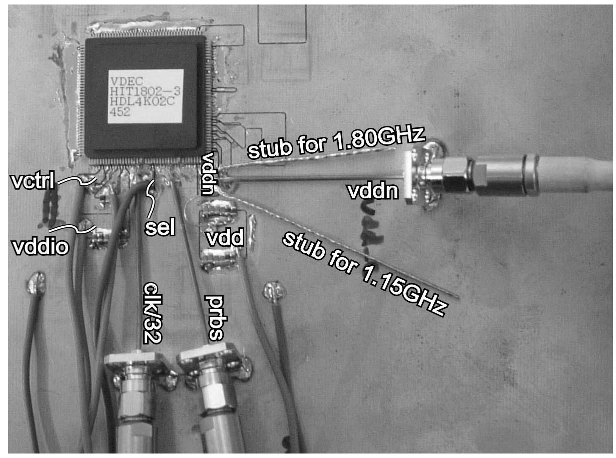

Fig. 3. Photograph of the chip mount, and the stubs.

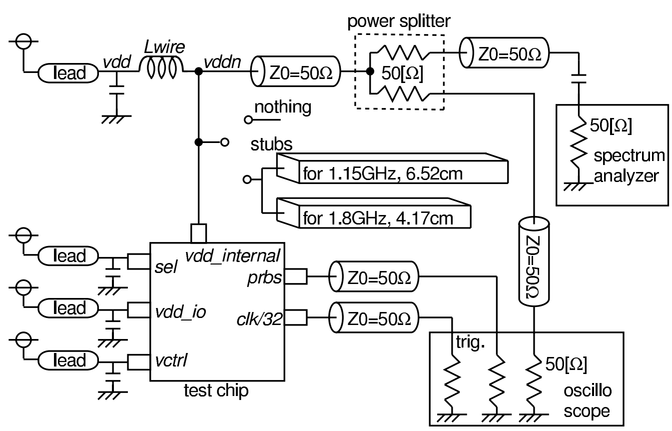

Fig. 4. Schematic of the measurement setup

Measurement Results

A. Spectra

Fig.5 shows the measured spectrum of the power supply noise of the repeat mode at the 1.15GHz operation with/without the stubs. This graph shows that the dominant noise frequency is the operating frequency, and the stub eliminates 91% of the 1.15GHz noise component.

The spectrum of the random mode are shown in Fig.6(i). Even though the noise is spread around the operating frequency because of its PRBS pattern, the stub suppresses the noise peak around 1.15GHz by 90%.

The measured waveforms of the *vddn* island on the random mode is shown in Fig.7. It shows that 48% of the total noise is reduced by the stub. The total noise value here is defined by the standard deviation σ from the average voltage V_{av},

$$V_{av} = \frac{1}{N}\sum_{i=1}^{N} V_i, \quad \sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(V_i - V_{av})^2} \qquad (5)$$

where N is the number of the sampling point which is 4096, and the sampling time step is constant in this experiment.

The total noise of the random mode is not completely suppressed because of the lower frequency component, while 83% of the total noise is reduced on the repeat mode whose lower frequency component is small as shown in Fig.5.

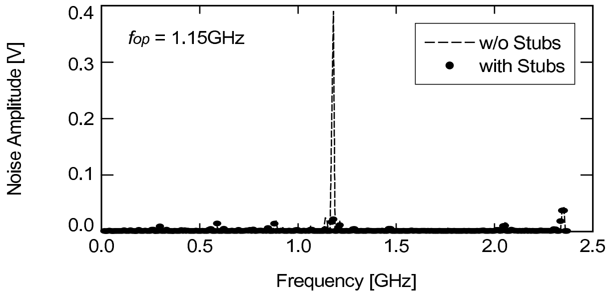

Fig. 5. Measured spectrum of the repeat mode at 1.15GHz operation, with/without the stubs.

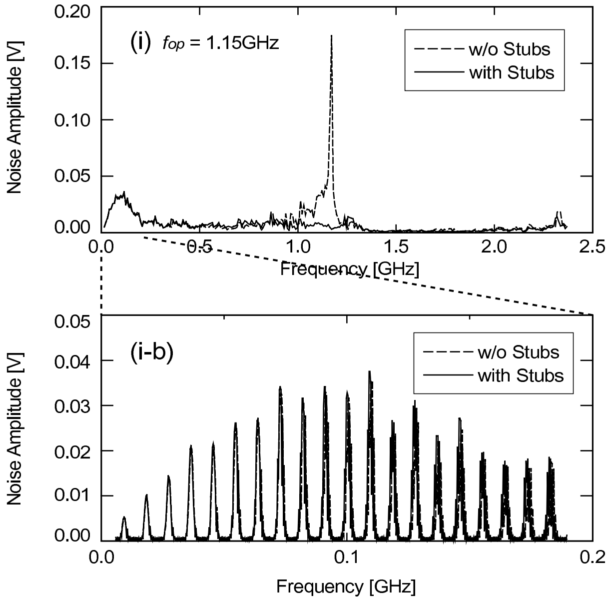

Fig. 6. Measured spectrum of the random mode at 1.15GHz operation, with/without the stubs. (i-b) The magnified graph of the lower frequency.

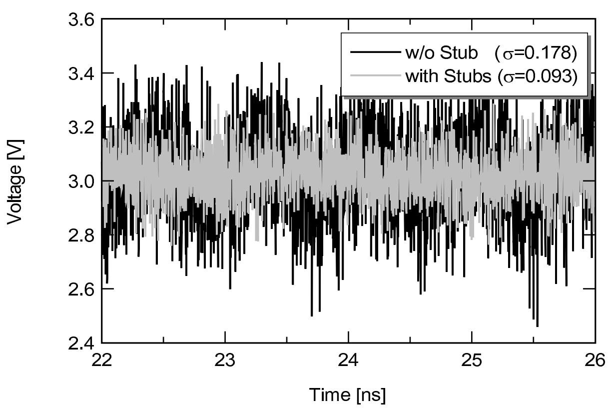

Fig. 7. Measured power supply noise waveform with and without stubs at 1.15GHz operation of the random mode.

B. Operating Frequency Dependence

The operating frequency dependence of the measured spectrum of the random mode is shown in Fig.8. The noise amplitudes of the operating frequency component with/without the stub have the same peaks in case (ii), (v), no peaks in case (iii), have different peaks in case (i), (iv).

Fig.9(a) shows the operating frequency dependence of the noise amplitude of the operating frequency component, and (b) shows the operating frequency dependence of the total noise (σ) defined as eqn(5), with the line of the case (i)-(v) frequencies. Both graphs are the measurement results of the random mode operation.

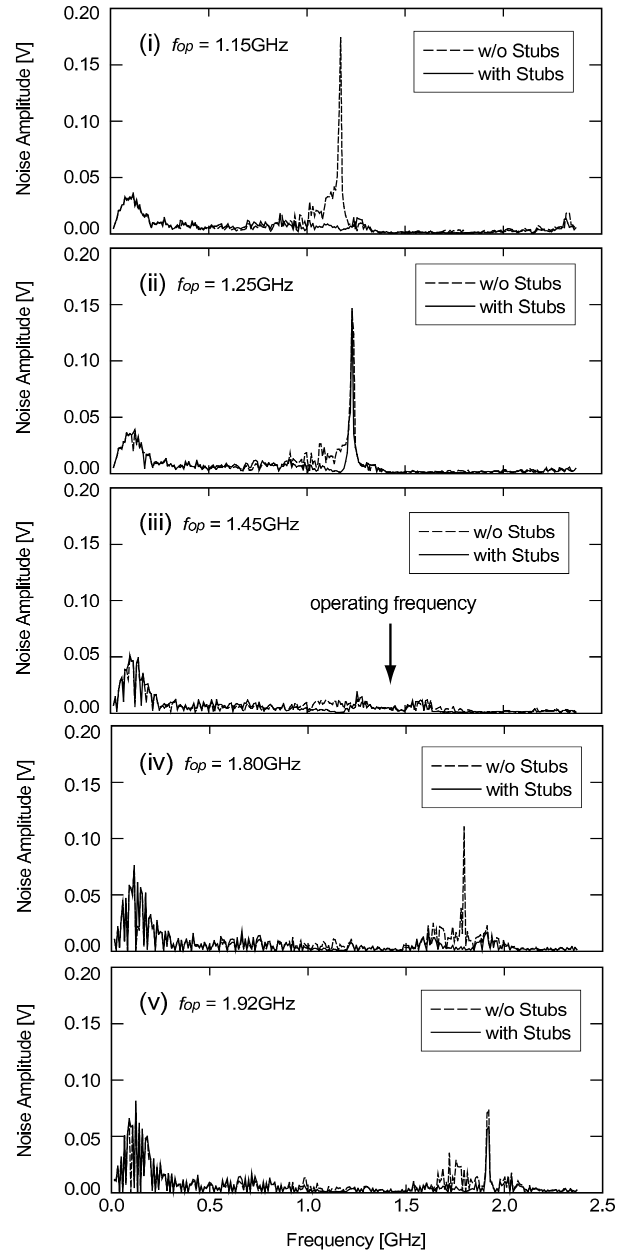

Fig. 8. Operating frequency dependence of the Random mode spectrum (measured).

The graph (a) indicates that the stubs for 1.15GHz, 1.80GHz remove 90%, 84% of the designed frequency noise, in case (i), (iv), respectively. The total noise reduction ratio of with/without stubs are 48% in case (i) while only 15% in case (iv), as shown in Fig.9(b), because the operating frequency component is the dominant noise in case (i) while case (iv) has some amount of power in lower frequency component which cannot be removed by the stubs, as shown in Fig.8(i) and (iv).

Fig.9 also indicates that at the frequencies other than the stubs adjusted, the noise amplitudes are similar for with/without stubs, in case (ii), (iii) and (v).

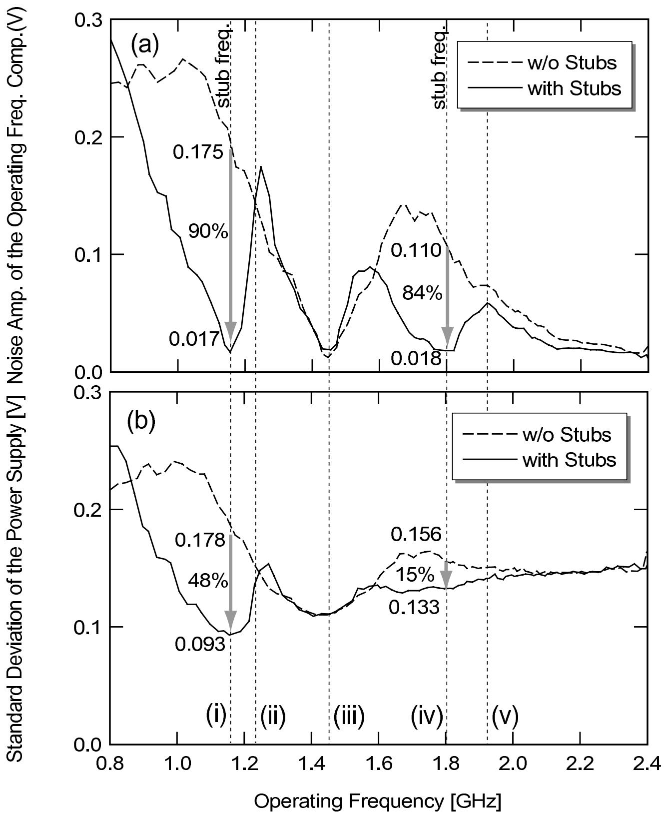

Fig. 9. Operating frequency dependence of the power supply noise in repeat mode. (a) Noise amplitude of the operating frequency component. (b) Total noise amplitude.

Discussion

A. Lower Frequency Noise

As shown in Fig.8, the power supply noise spectrum have some amount of power in lower frequency components. The PRBS 2^7-1 circuit generates pseudo-random bit pattern which repeats in every $2^7-1 = 127$ clock cycles, and the stream has 1.15GHz/127 = 9.06MHz component as the basic frequency. Fig.6(b) shows that the lower frequency set are the harmonics of the basic frequency. It means that these noises are caused by the PRBS 2^7-1 stream characteristics.

B. Operating Frequency Dependence

As being discussed in the previous section, the stubs remove the noise of the designed frequencies. In case (iii), however, the noise amplitude of the operating frequency is suppressed even though the frequency is not the frequencies of the stubs, as shown in Fig.8(iii) and Fig.9(a). This is because of the package and bonding wire frequency characteristics. The transistor switchings occur inside the LSI package, and the impedance of the package and bonding wire is large enough at the frequency that the noise does not come out from the package. Thus, the noise of the frequency is not observed.

C. Possibility for On-chip Stubs

The stub length is in inverse proportion to the operating frequency, as expressed by eqn(4), and the dielectric constant becomes 3.9 if the stubs are integrated on-chips because the stubs stay in SiO_2. Fig.10 shows the prediction of the required stub length based on the ITRS roadmap of MPU clock frequency[4]. It shows that the stub length will be shortened to about 5mm in 2007, and on-chip stubs will be possible.

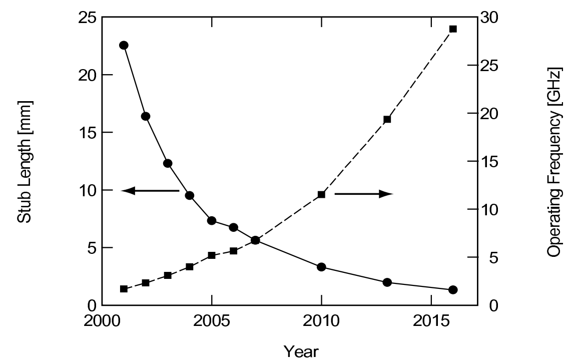

Fig. 10. ITRS roadmap of MPU clock frequency, and corresponding stub length.

Conclusion

We have demonstrated the power supply noise reduction using stubs. A quarter-length stub attached to the power supply line of an LSI chip works as a band-eliminate filter, and suppresses the power supply noise of the designed frequency. The measurement results show that 90% of the designed frequency noise component and 48% of the total noise are reduced when the stubs are attached to a 1.15GHz operating test chip which has a PRBS generator with inverter chains. These results show the possibility of the stub on-chip integration which can eliminate the package and bonding wire parasitic impedance effects when the chip operating frequency becomes higher and the stub length becomes shorter.

Acknowledgement

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Hitachi Ltd. and Dai Nippon Printing Corporation. This study was supported by Grant-in-Aid for JSPS Fellows of the Ministry of Education, Culture, Science and Technology.

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